

Enrico Caruso 14

Muxless Schematics Document

Ivy Bridge & Sandy Bridge

Intel PCH

2012-01-03

REV : X02

DY : None Installed
PSL: 10mW internal schematic
UMA: UMA ONLY installed
OPS: Optimus solution installed.
Surge: For GO Rural config stuff.
GIGA: For GIGA LAN config stuff.
LPC : Reserve for LPC debug card
POP : Reserve for solve "POP" sound issue

Project code:

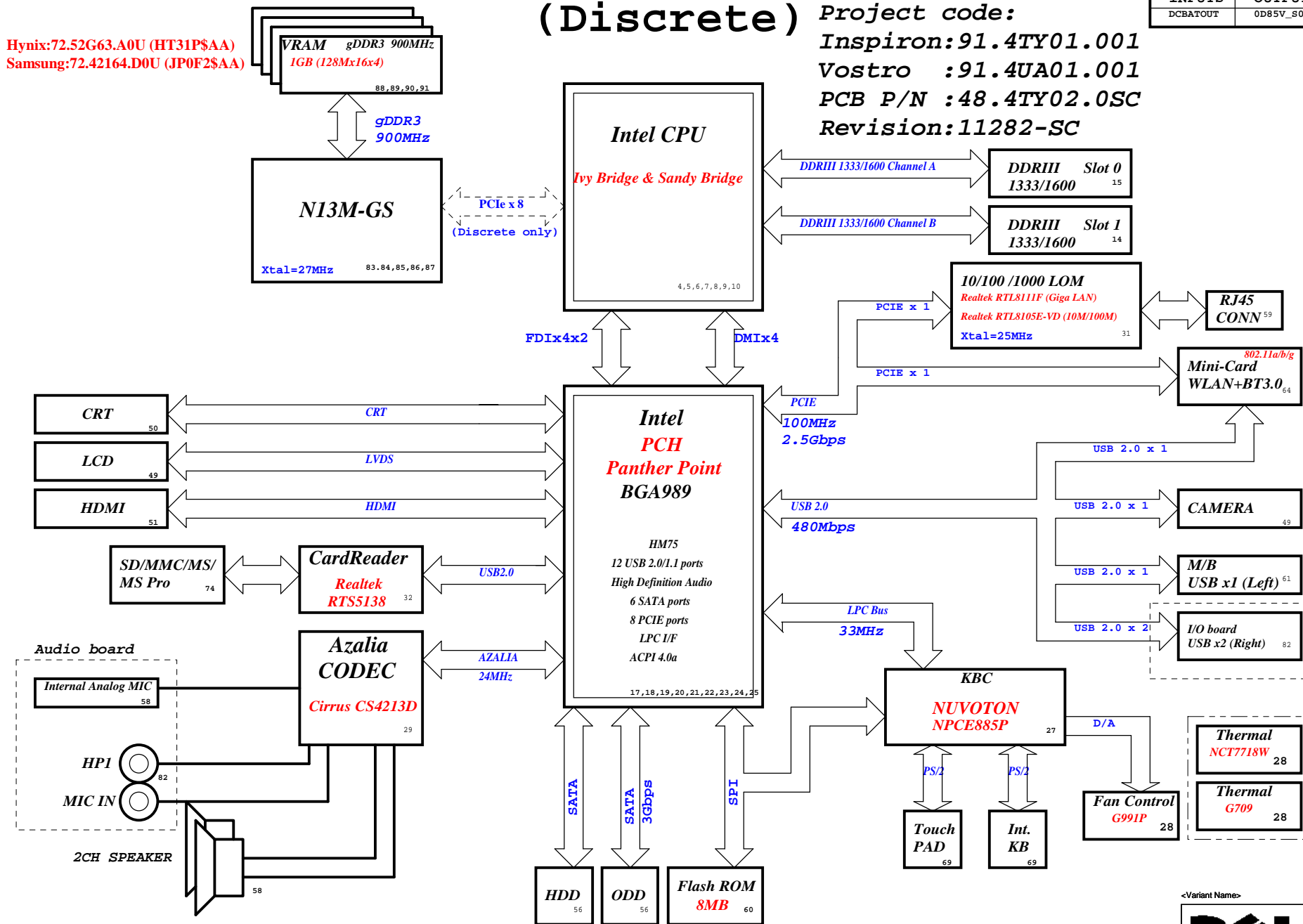
Inspiron:91.4TY01.001
Vostro :91.4UA01.001
PCB P/N :48.4TY02.0SC
Revision:11282-SC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Block Diagram
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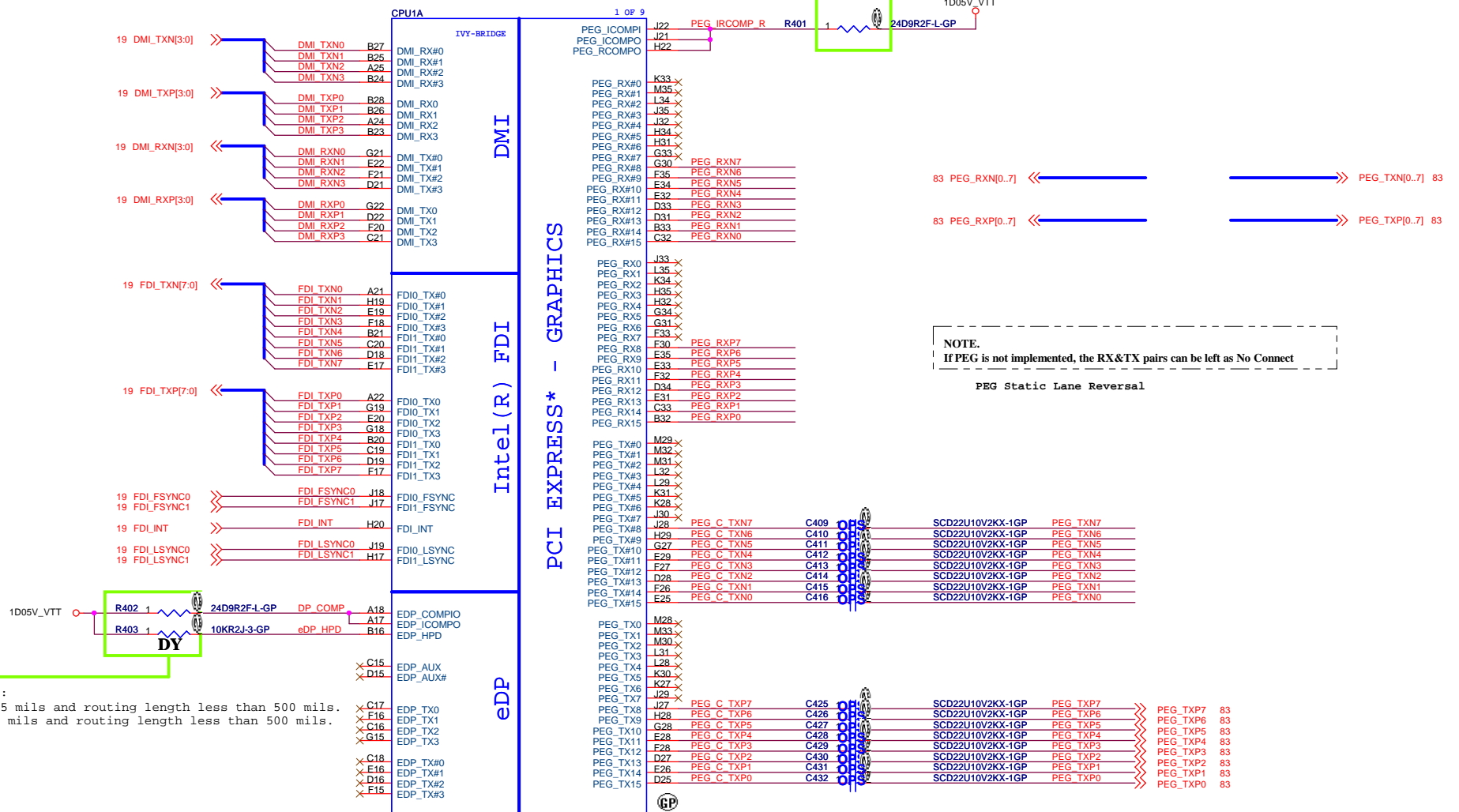
Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Friday, December 30, 2011	Sheet 2 of	104

WWW.AliSaler.Com



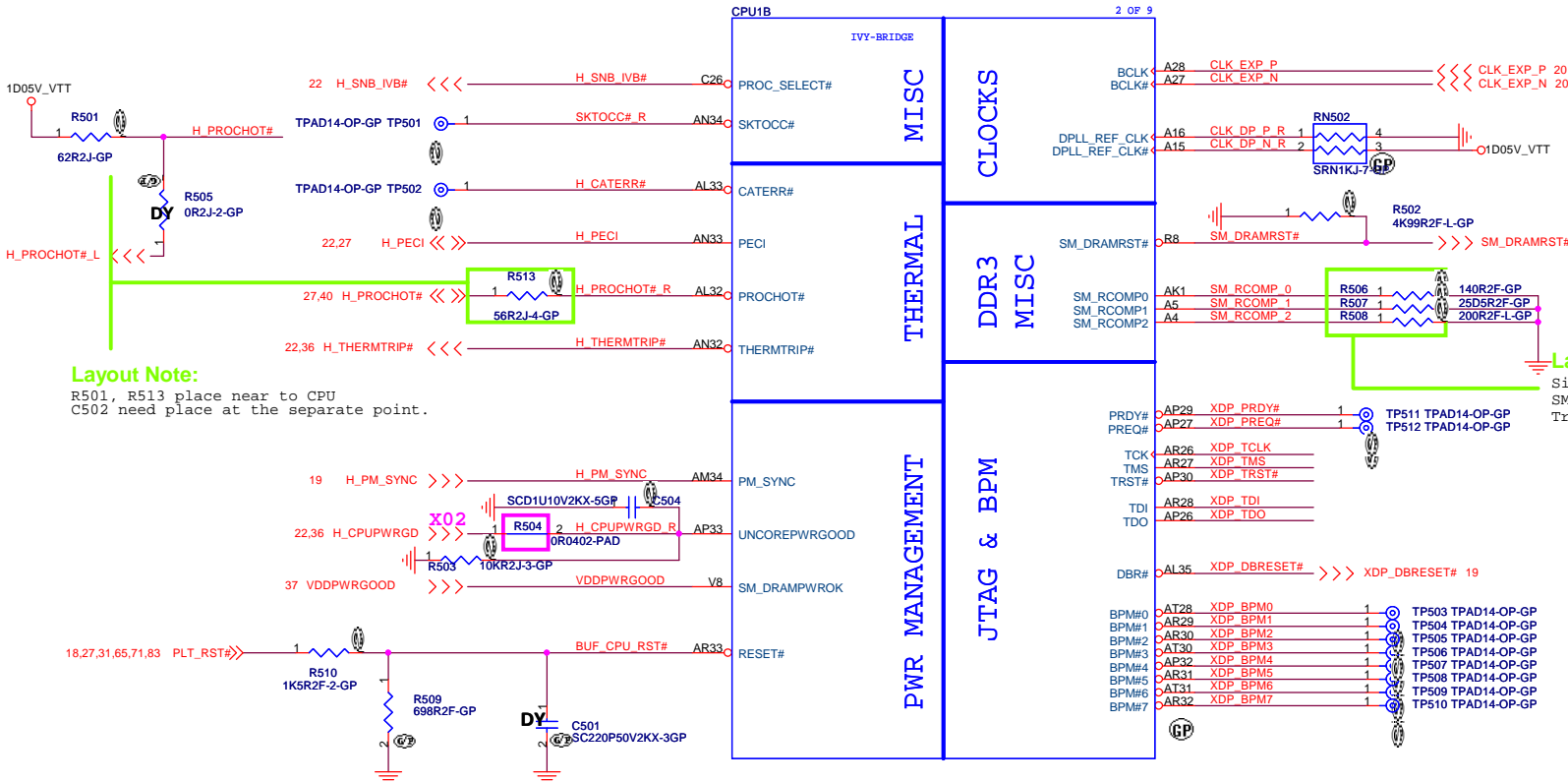
Layout Note:

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



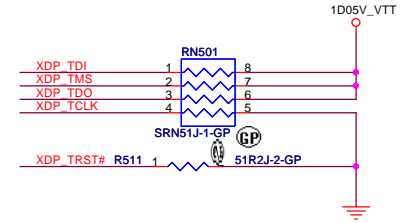
<Variant Name>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU (PCIE/DMI/FDI)			
Size	Document Number	Rev	
A3	Enrico Caruso 14 MLK DIS	X02	
Date:	Tuesday, January 03, 2012	Sheet	4 of 104



Layout Note:
R501, R513 place near to CPU
C502 need place at the separate point.

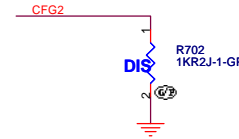
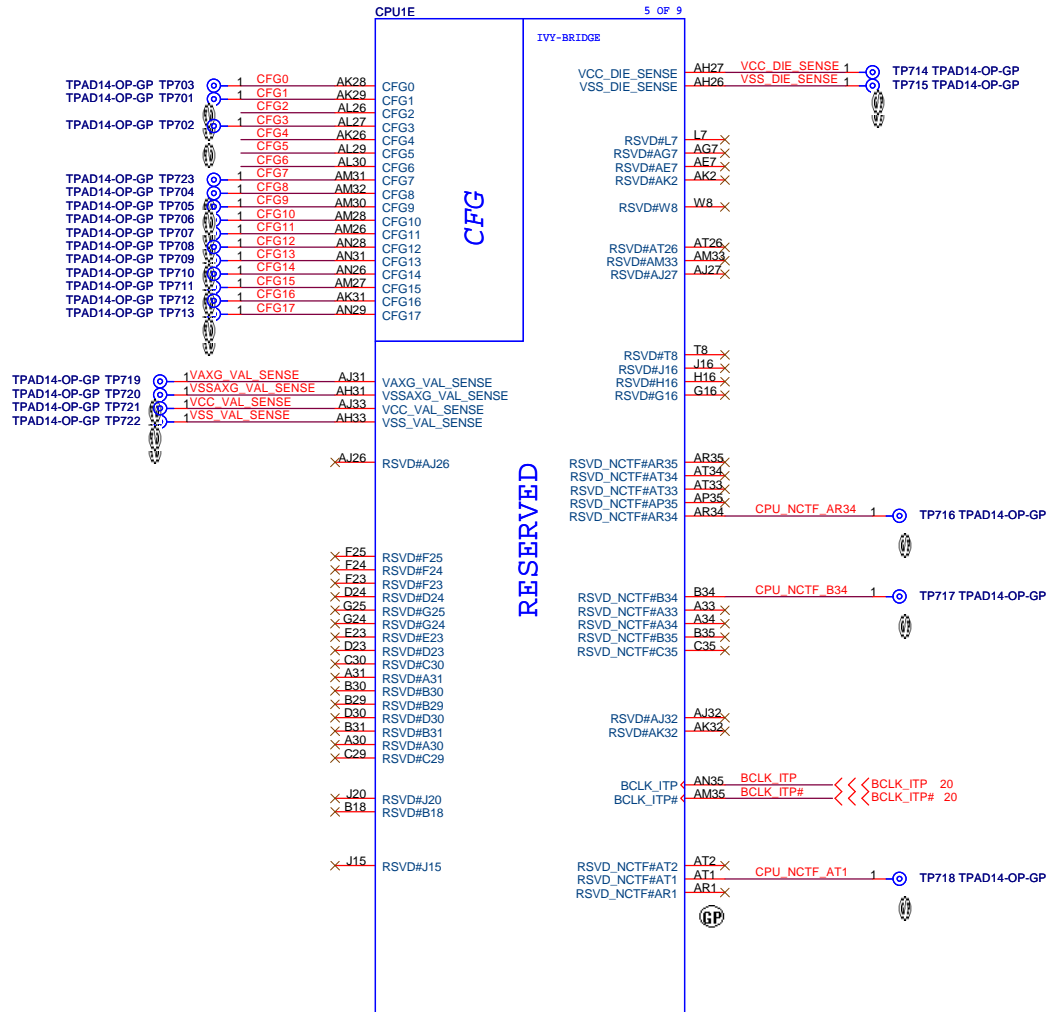
Layout Note:
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil



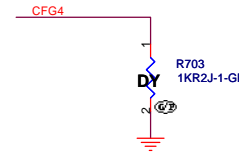


104

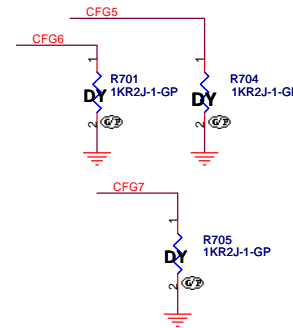
SSID = CPU



PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

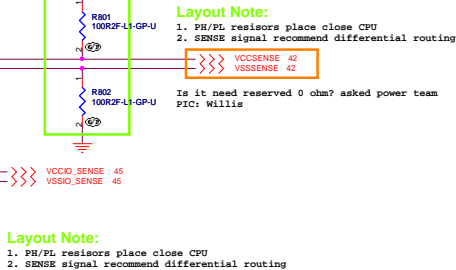
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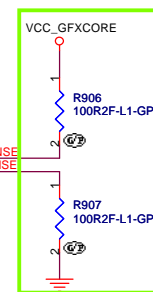


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CPU (RESERVED)		
Title	Document Number	Rev
	Enrico Caruso 14 MLK DIS	X02
Date: Tuesday, January 03, 2012	Sheet 7	of 104

Refer to PDDG rev 0.8





Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(DC)	0.3~1.35	53
VAXG(DC)	0~1.3	33
VCCIO	1	8.5
VDDQ	1.5	10
VCCSA	0.9	6
VCCPLL	1.8	1.5

Refer to PDDG rev 0.8

Layout Note:

1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

VCCSA Output Decoupling Recommendation:
 1 x 330 uF, 6m
 2 x 10 uF at Bottom Socket Cavity
 1 x 10 uF at Bottom Socket Edge

Do not have 1 x 330 uF

R910 close to pin H23.

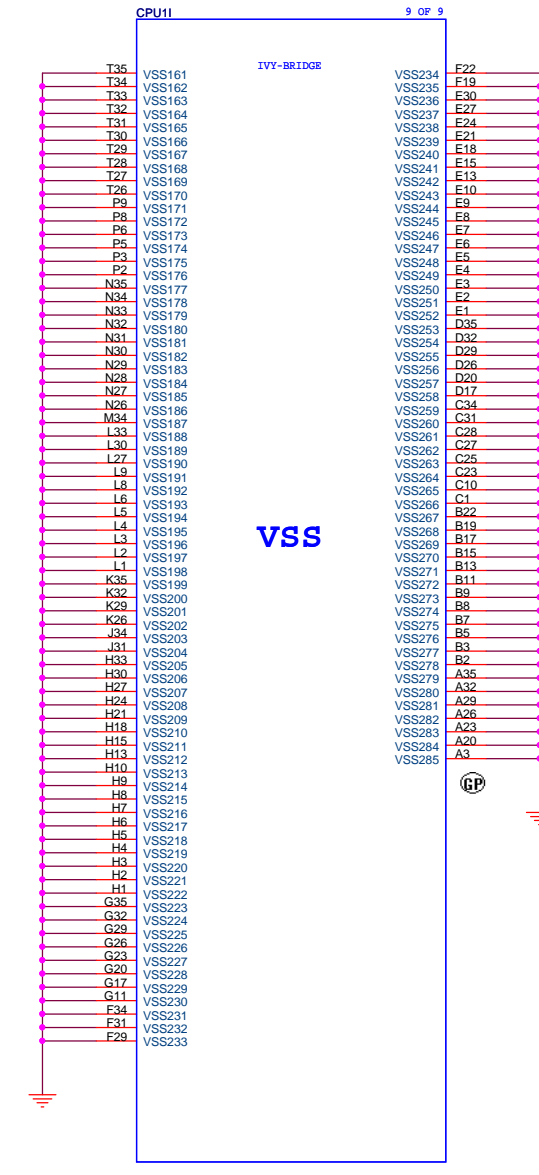
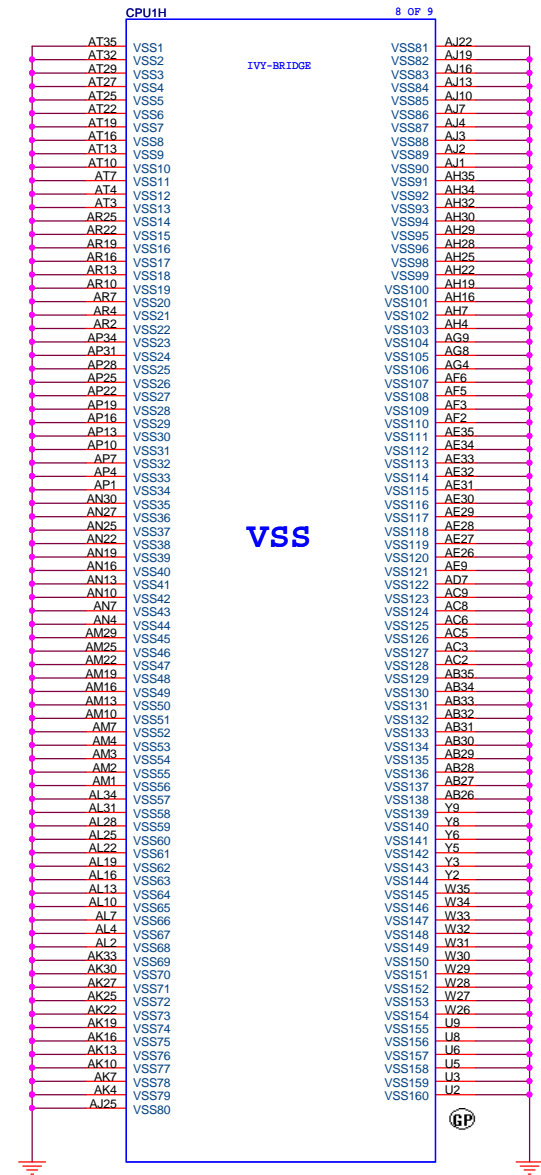
VCCSA Power Select		
Voltage(V)	VID[0]	VID[1]
0.9	0	0
LV & ULV 0.85	0	1
Others 0.8		
0.725	1	0
0.675	1	1

<Variant Name>



Title **CPU (VCC GFXCORE)**

Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Tuesday, January 03, 2012	Sheet 9 of 104	



<Variant Name>

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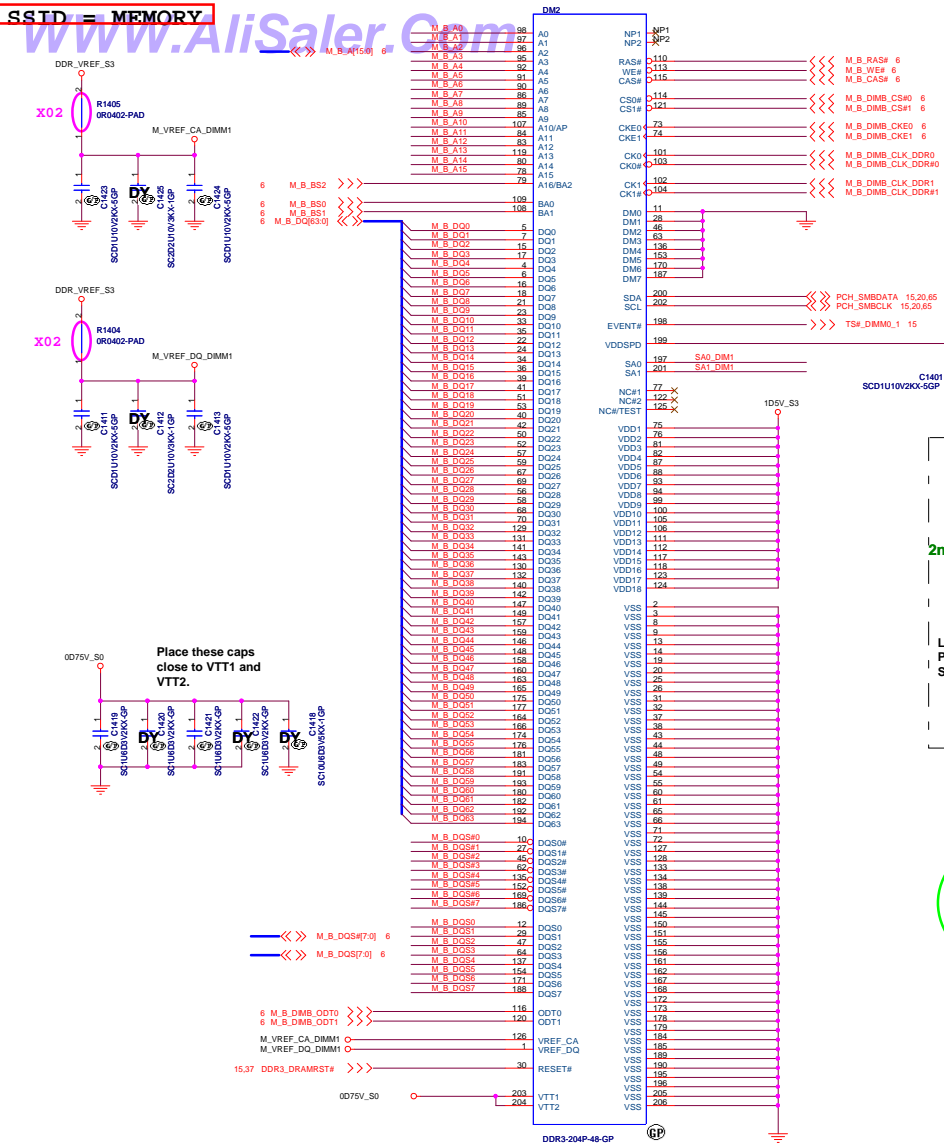
Title

CPU (VSS)

Size A3 Document Number Rev

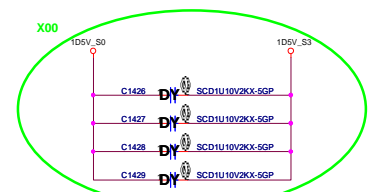
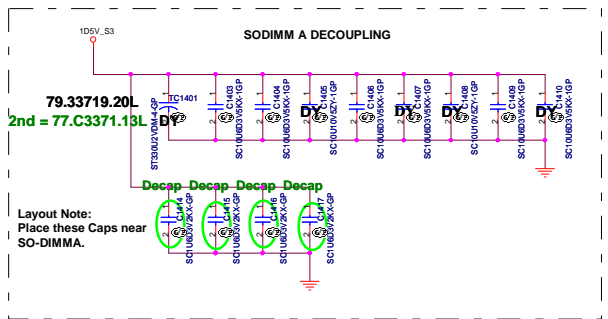
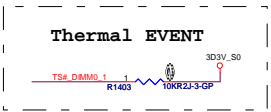
Enrico Caruso 14 MLK DIS **X02**

Date: Friday, December 30, 2011 Sheet 10 of 104

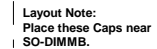
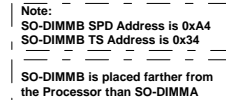


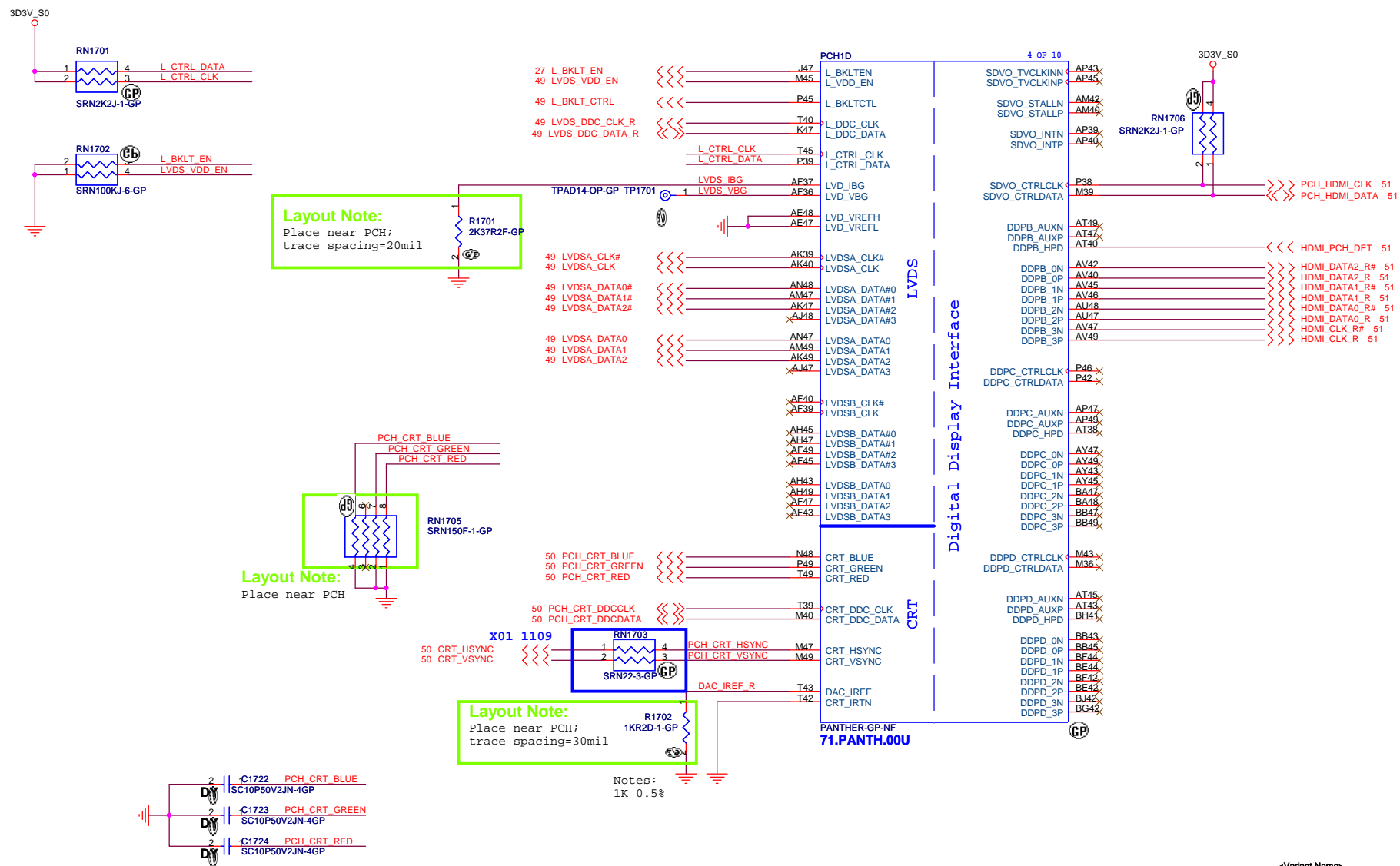
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

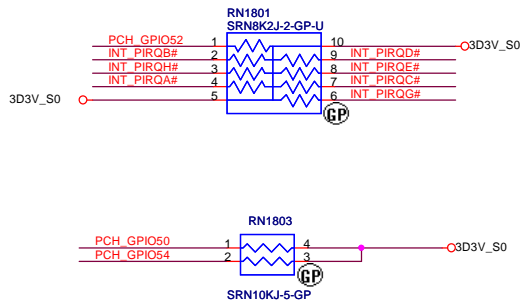
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Layout Note:
For S3 reduction circuit's 1D5V return pass.







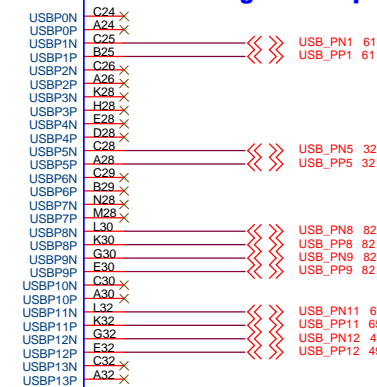
USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB Table

Pair	Device
0	NC
1	USB2.0 port1
2	NC
3	NC
4	NC
5	Card reader
6	NC
7	NC
8	USB2.0 port2
9	USB2.0 port3
10	NC
11	Mini Card1
12	CAMERA
13	NC

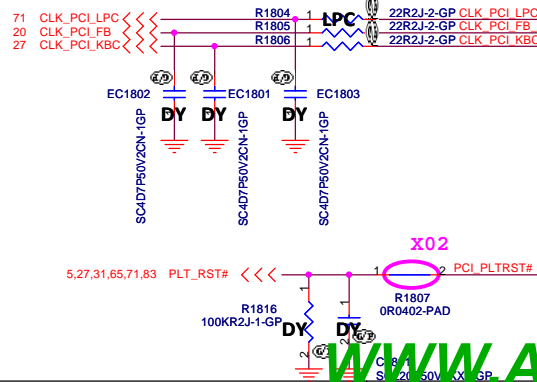
USB2.0 Signal Group



Layout Note:

1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



Al6 Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default

<Variant Name>

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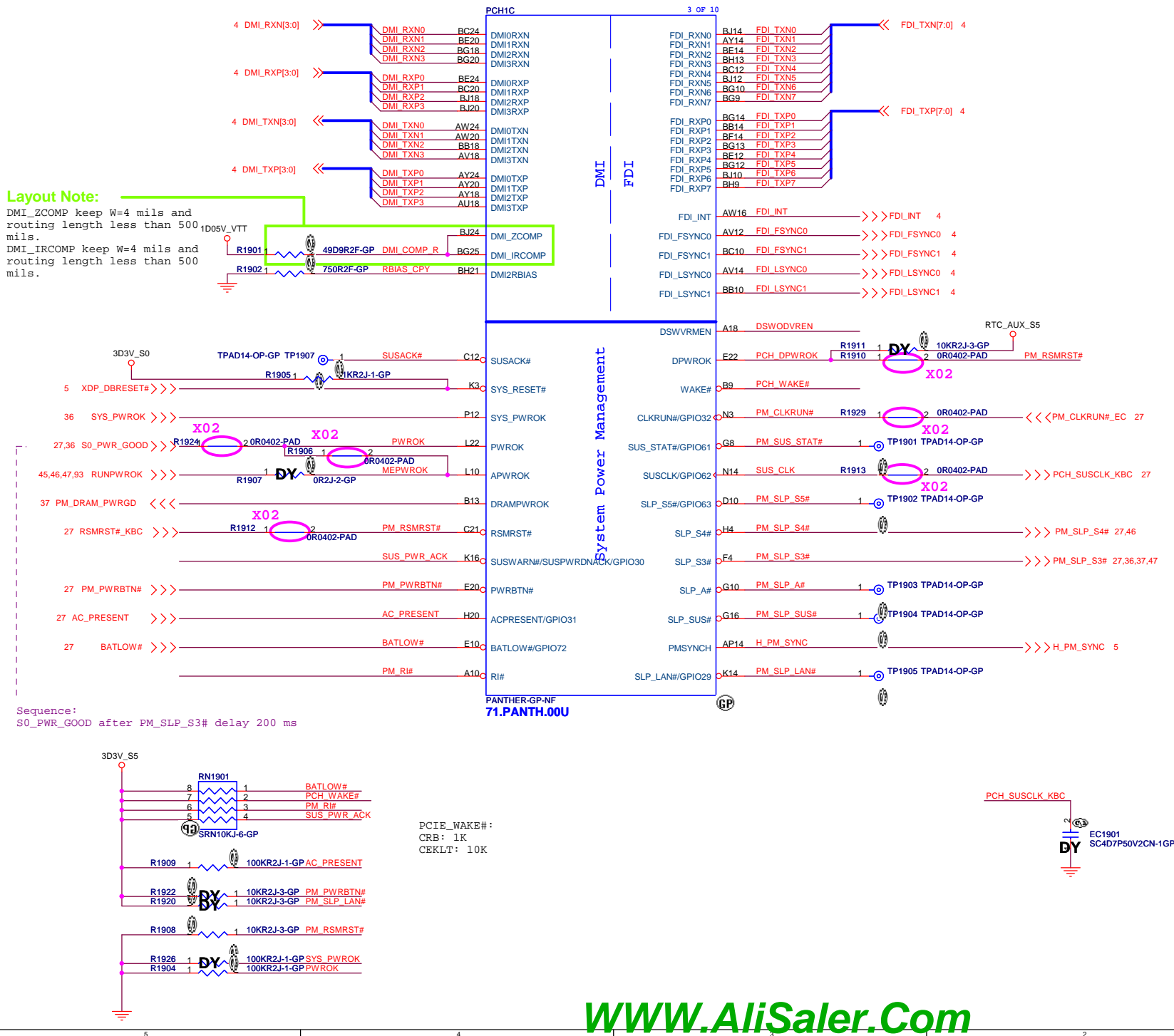
Title: **PCH (PCI/USB/NVRAM)**

Size A3 Document Number: **Enrico Caruso 14 MLK DIS** Rev: **X02**

Date: Tuesday, January 03, 2012 Sheet 18 of 104

Layout Note:

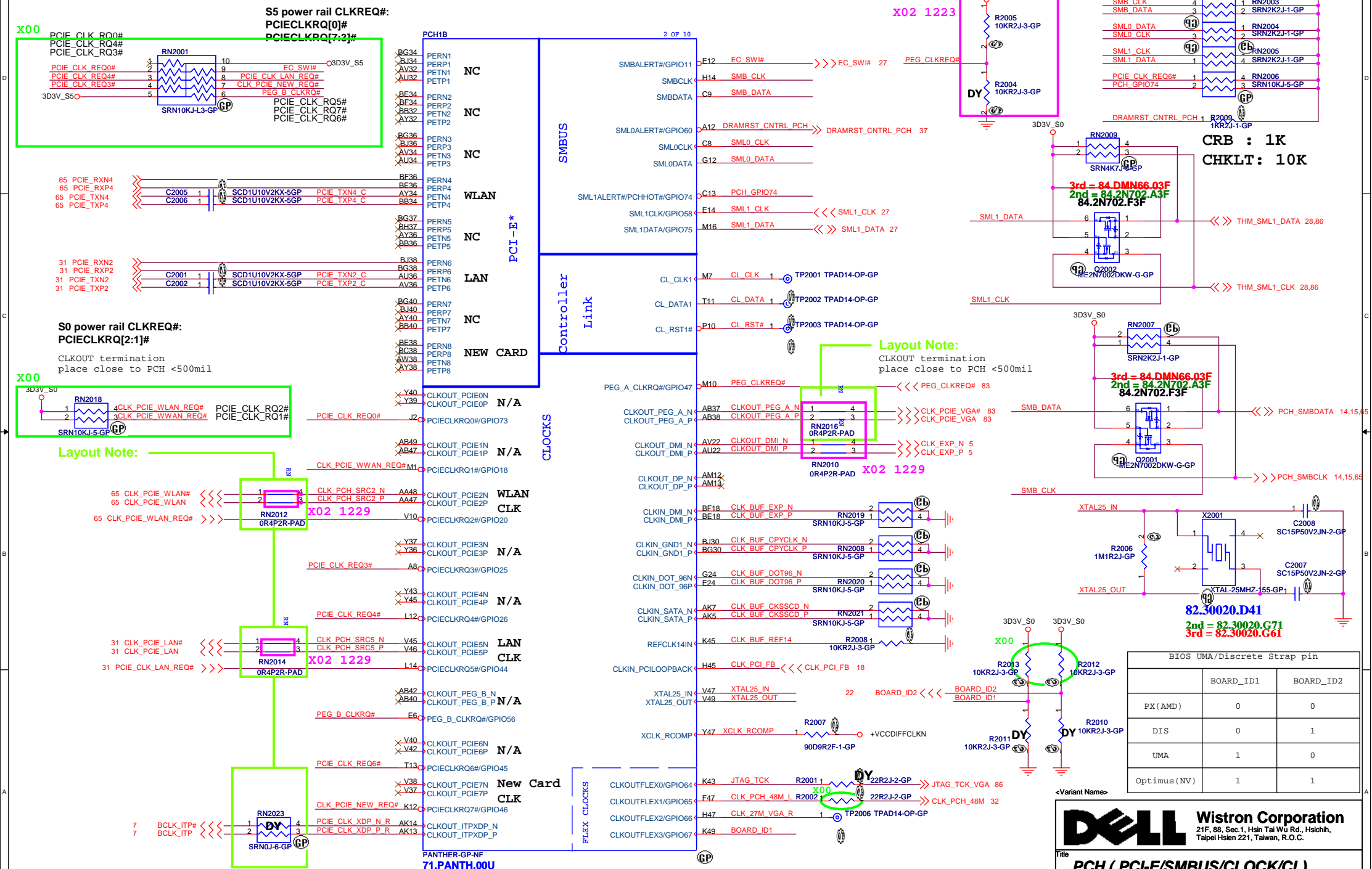
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

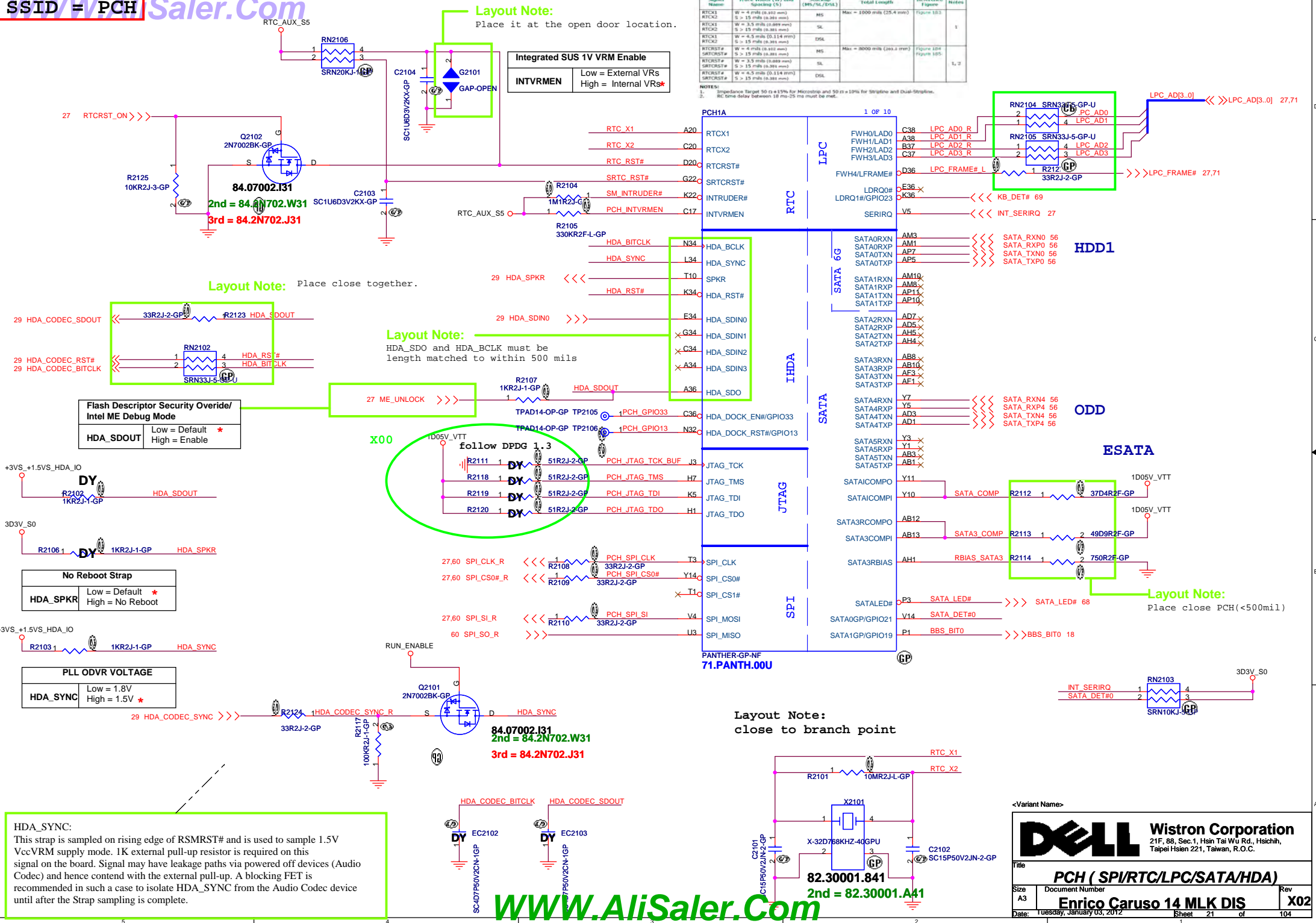


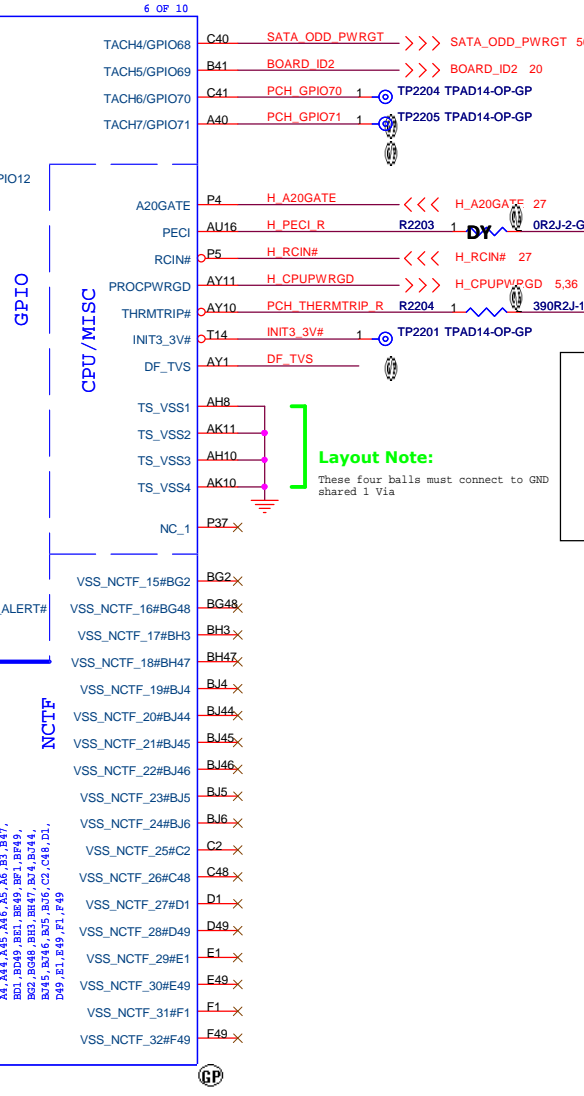
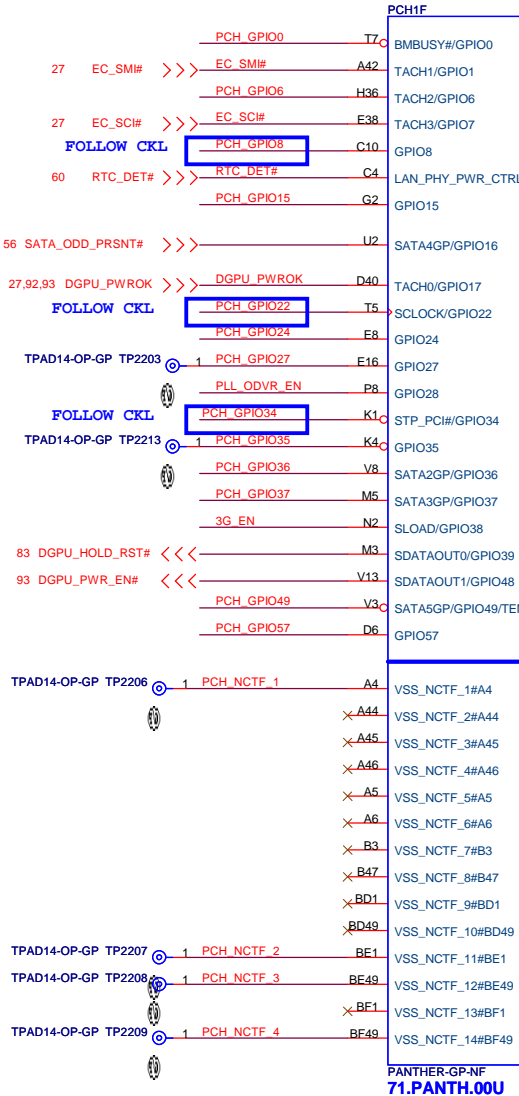
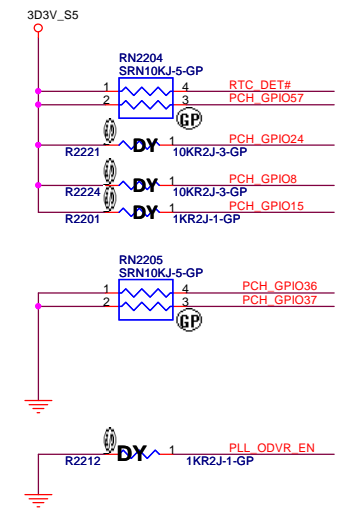
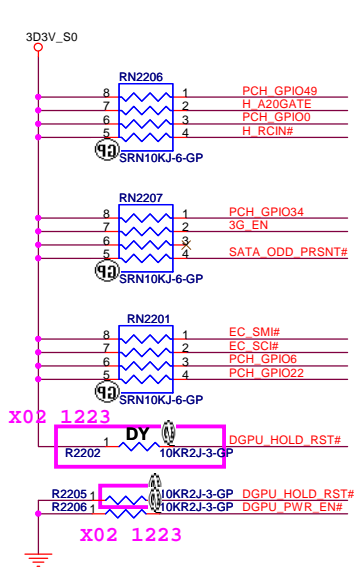
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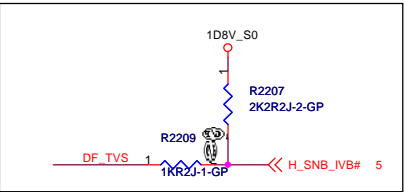
Title: **PCH (DMI/FDI/PM)**
Size: A3 Document Number: **Enrico Caruso 14 MLK DIS** Rev: **X02**
Date: Tuesday, January 03, 2012 Sheet 19 of 104







Layout Note:
These four balls must connect to GND shared 1 Via



PLL ON DIE VR ENABLE	
GPIO28 (PLL_ODVR_EN)	Weakly internal pull up 20k. High - Enable LOW - Disable

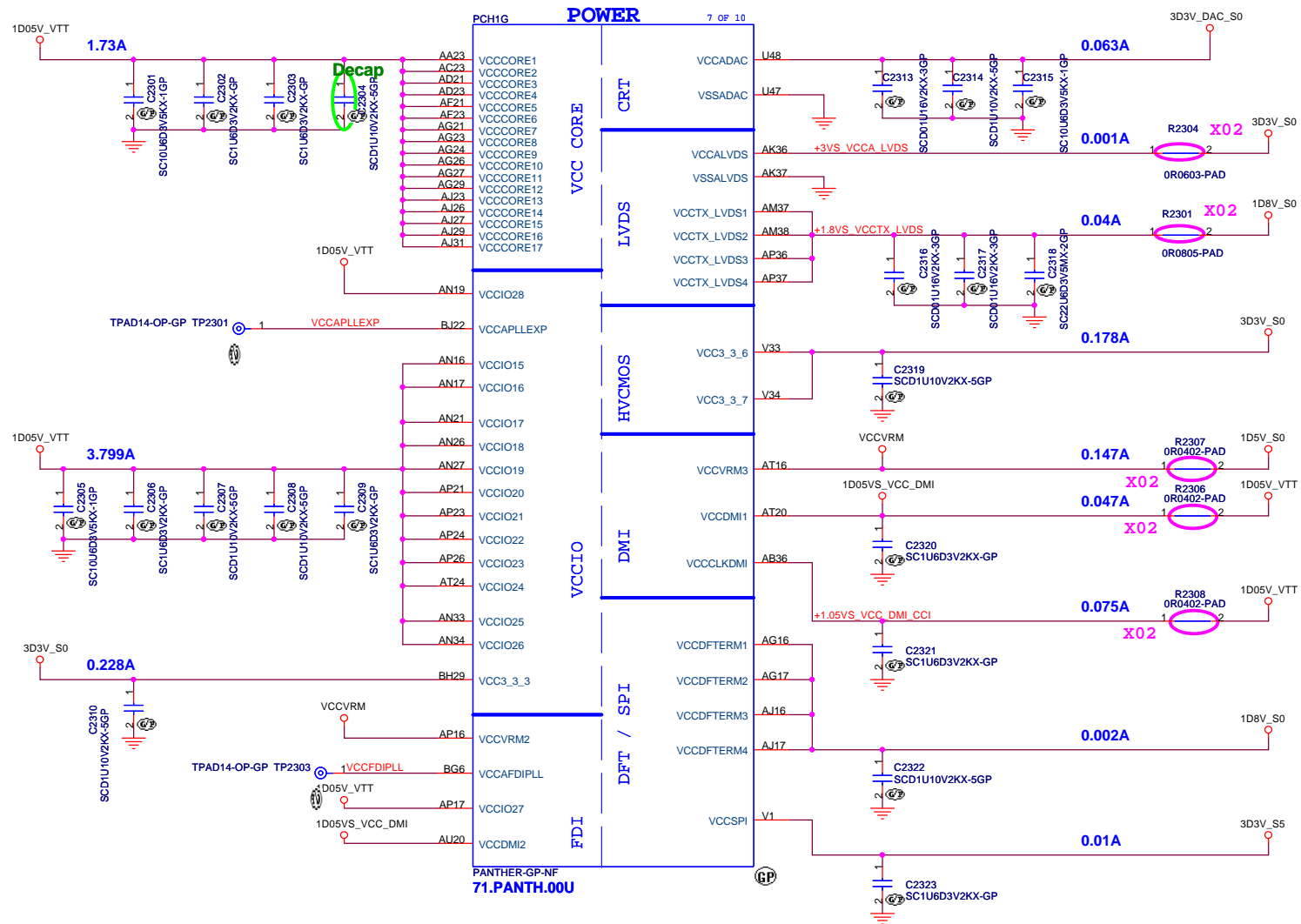
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DELL

Title: **PCH (GPIO/CPU)**

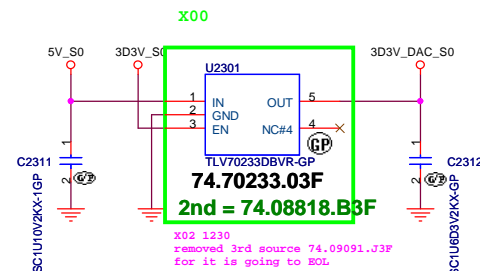
Size: A3
Document Number: **Enrico Caruso 14 MLK DIS**
Date: Tuesday, January 03, 2012

Rev: **X02**
Sheet: 22 of 104



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Refer to PCH EDS V1.5
(General DC Characteristicschipset)



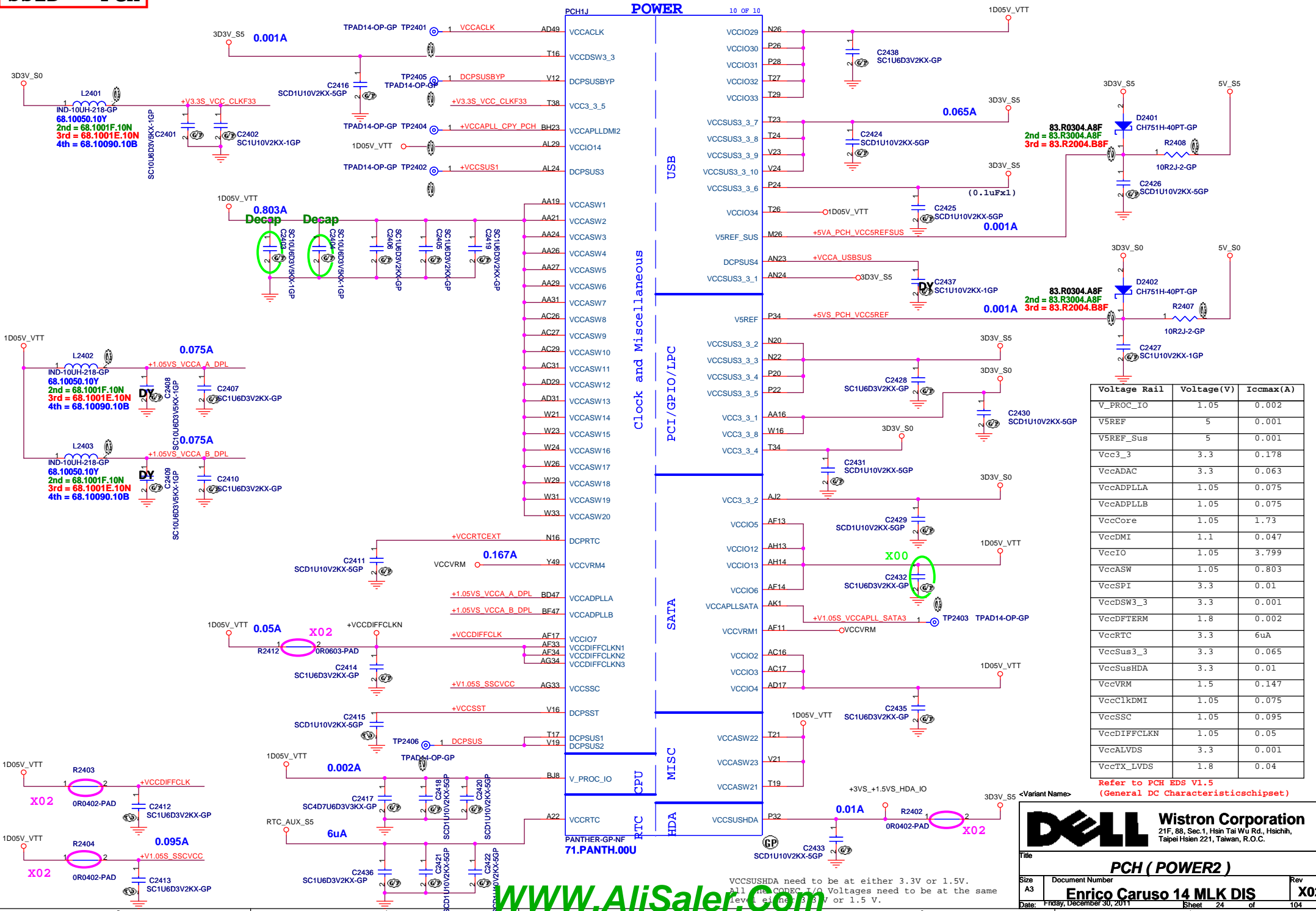
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Title: **PCH (POWER1)**

Size: A3 Document Number: **Enrico Caruso 14 MLK DIS** Rev: **X02**

Date: Friday, December 30, 2011 Sheet: 23 of 104



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDPTerm	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.05
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

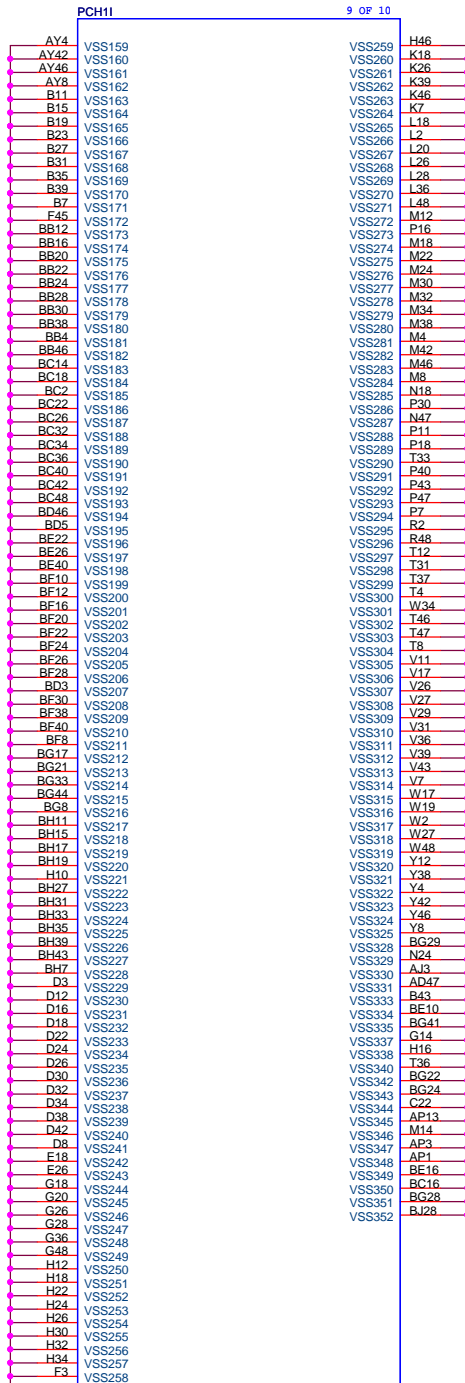
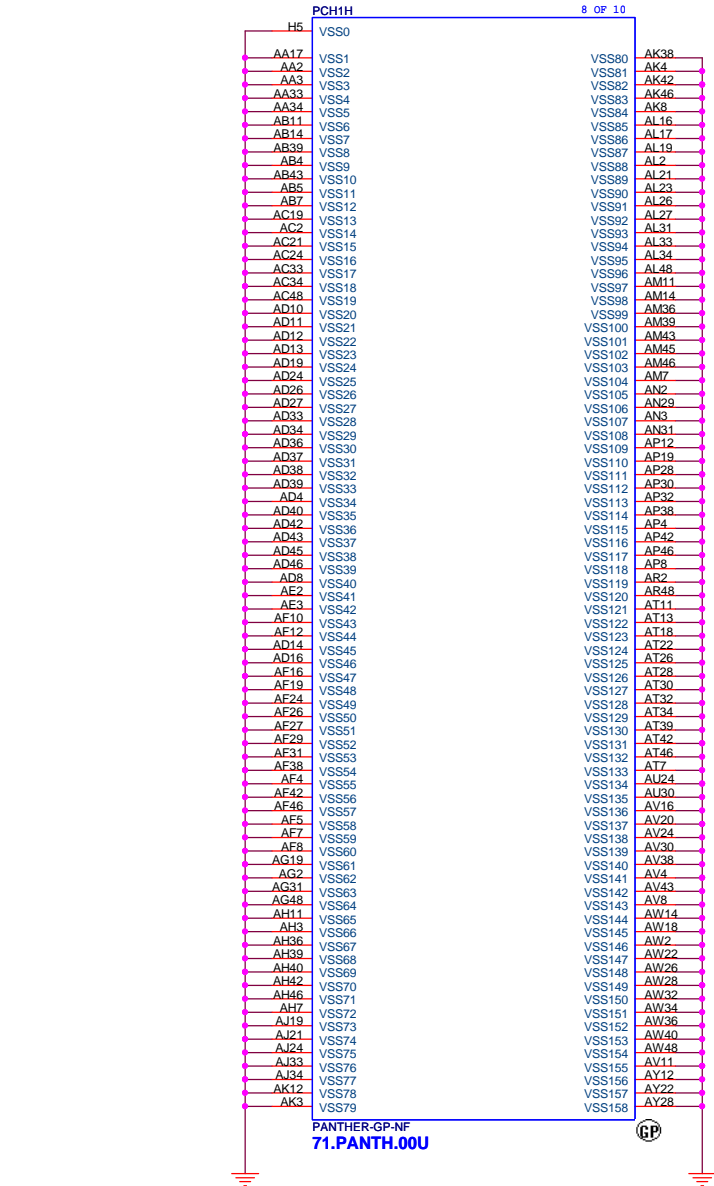
Refer to PCH EDS V1.5
(General DC Characteristicschipset)



Title **PCH (POWER2)**

Size A3	Document Number Enrico Caruso 14 ML K DIS	Rev X
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Date: Friday, December 30, 2011 Sheet 24 of 104



<Variant Name>

DELL Wistron Corporation
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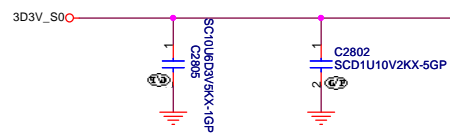
Title **PCH (VSS)**

Size A3 Document Number **Enrico Caruso 14 MLK DIS** Rev **X02**

Date: Friday, December 30, 2011 Sheet 25 of 104

SSID = Thermal

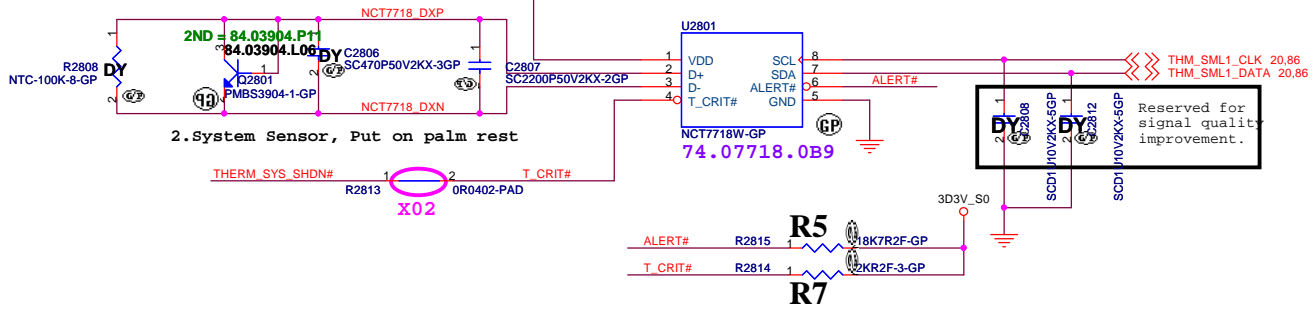
Thermal sensor NCT7718W



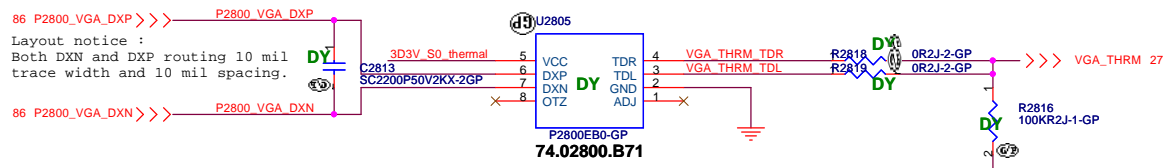
Alert# /T CRIT#		Pull-up Resistor	
R5	2Kohm	7.5Kohm	10.5Kohm
7.5Kohm	87°C	97°C	107°C
10.5Kohm	79°C	89°C	99°C
14Kohm	81°C	91°C	101°C
18.7Kohm	83°C	93°C	103°C
	85°C	95°C	105°C
			117°C
			119°C
			121°C
			123°C
			125°C

T_CRIT temperature strapping point

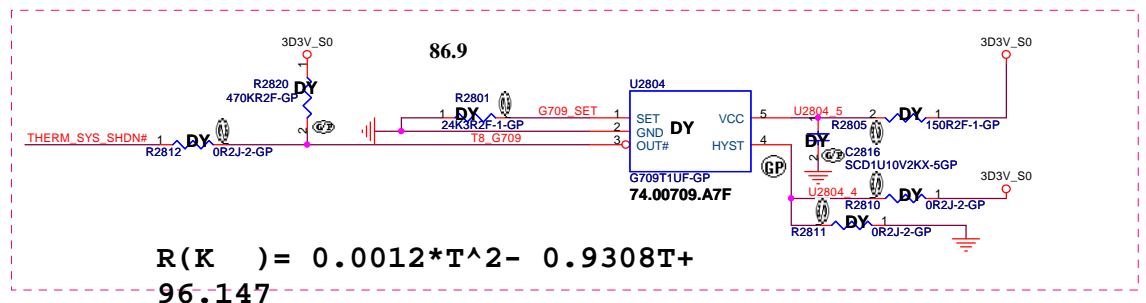
Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing. and route has to be away from the high noise area.
Put the C2807 2200pF to close the NCT7718W



VGA Thermal sensor P2800

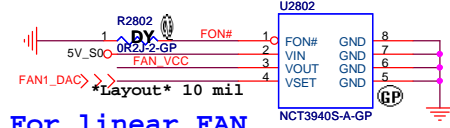


X02-0311 Add R2816& R2817 to
option VGA_THRM
and DY the circuit



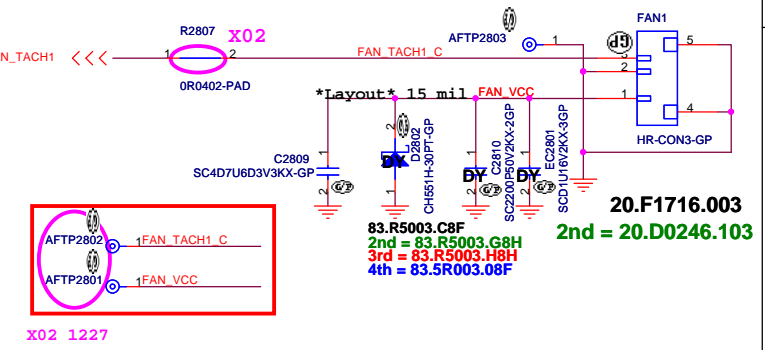
$$R(K) = 0.0012 * T^2 - 0.9308T + 96.147$$

Fan controller G991



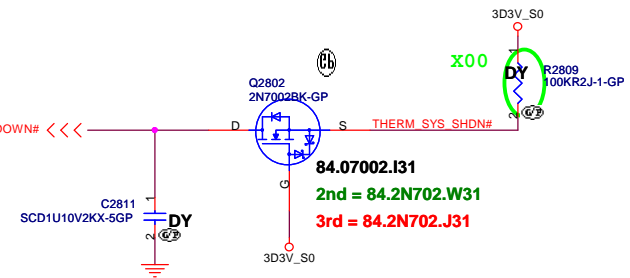
For linear FAN

74.03940.A71
2nd = 74.02793.A31
3rd = 74.00991.031



83.R5003.C8F
2nd = 83.R5003.G8H
3rd = 83.R5003.H8H
4th = 83.5R003.08F

20.F1716.003
2nd = 20.D0246.103



84.07002.I31
2nd = 84.2N702.W31
3rd = 84.2N702.J31

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Title

Thermal P2800/Fan Controller P2793

Size

Document Number

Rev

A3

Enrico Caruso 14 MLK DIS

X02

Date

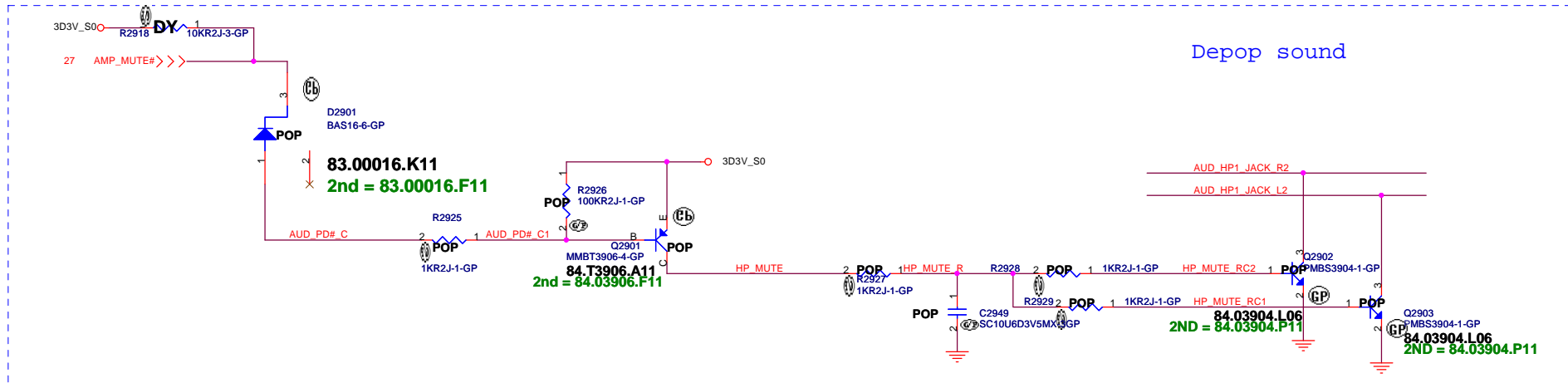
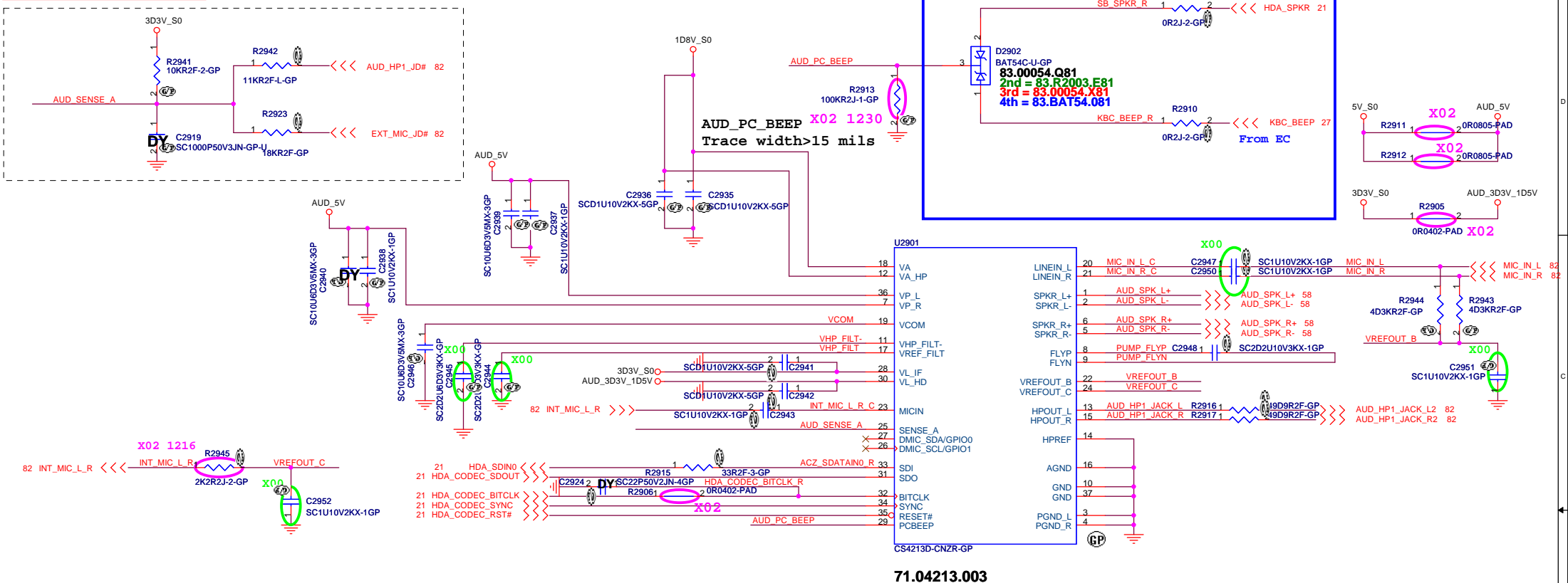
1 Tuesday, January 03, 2012

Sheet

28

of

104



<Variant Name>

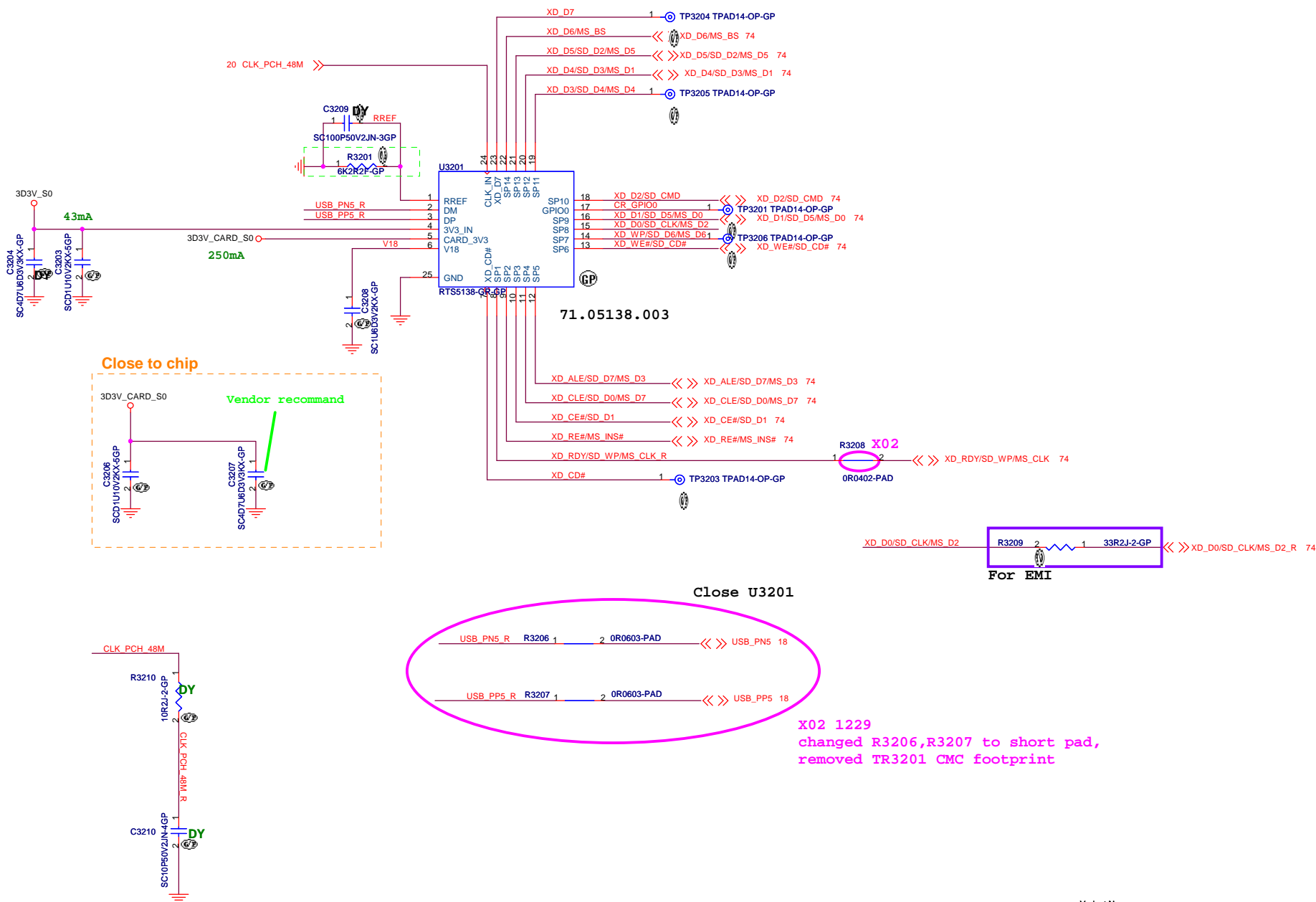
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Audio Codec CS4213D**

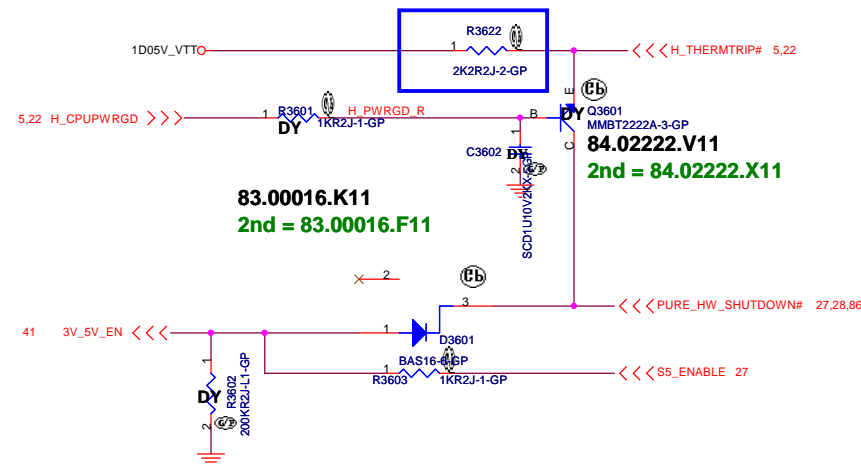
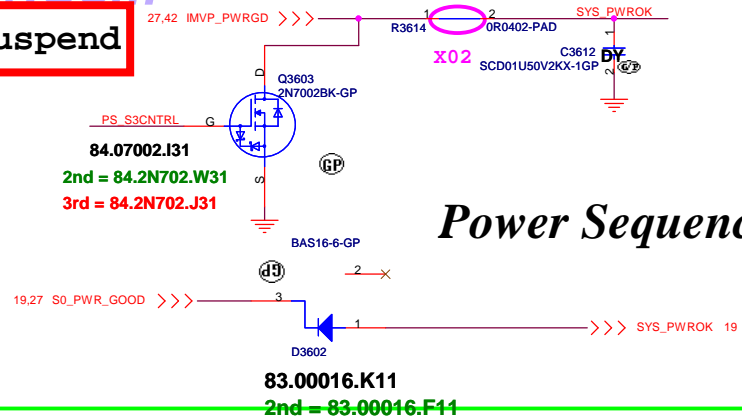
Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Tuesday, January 03, 2012	Sheet 29 of 104	

LAN CHIP

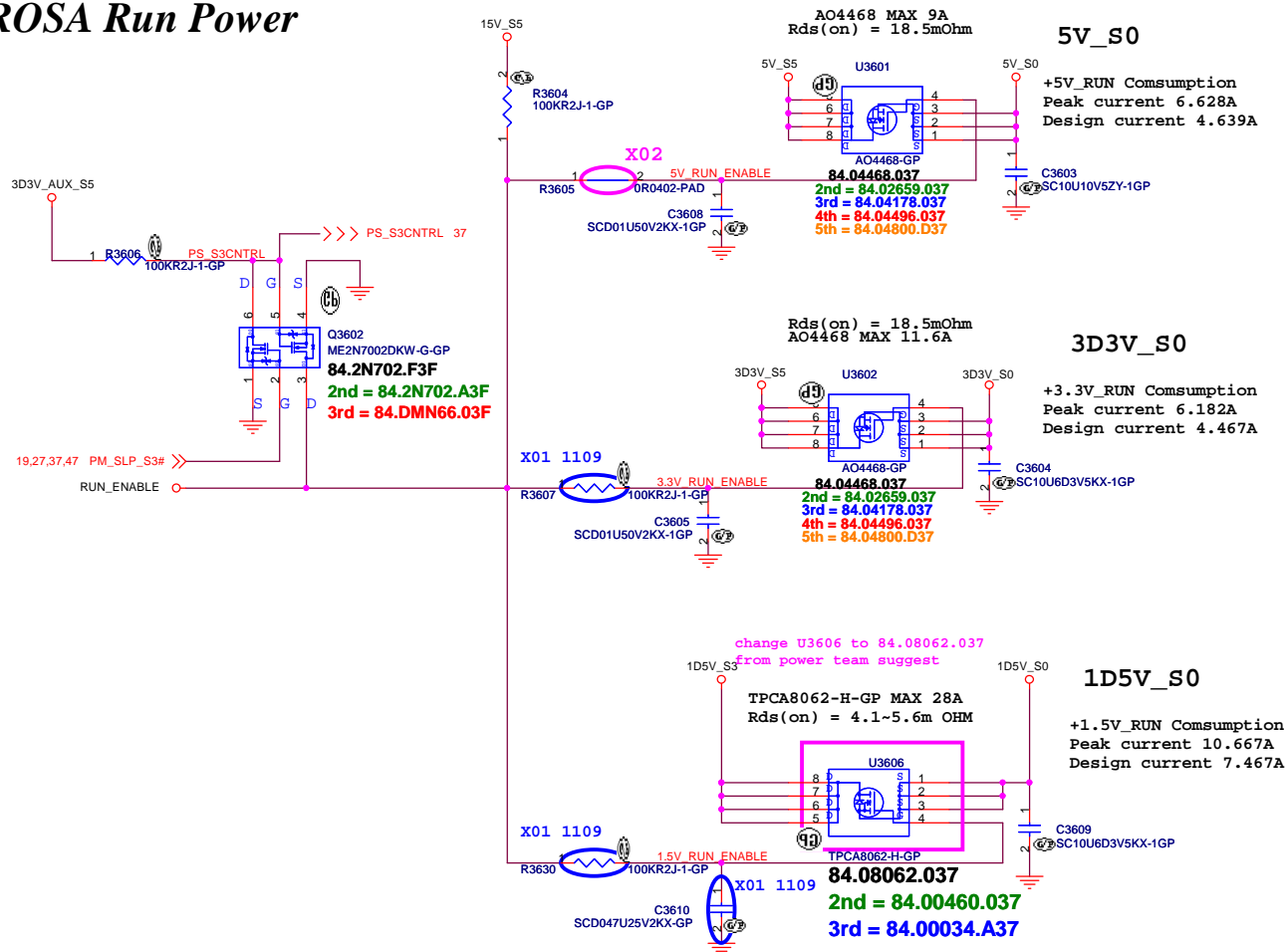
SSID = SDIO



SSID = Reset.Suspend



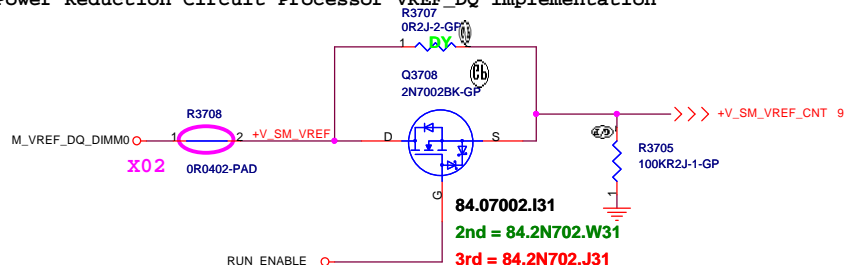
ROSA Run Power



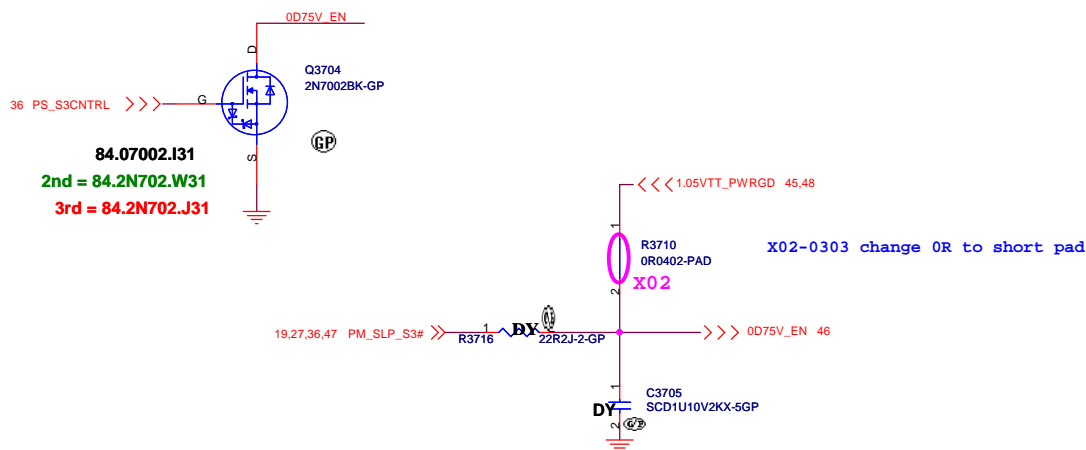
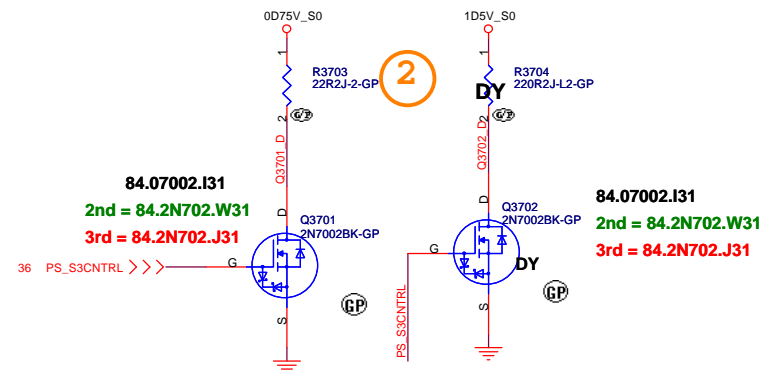
<Variant Name>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power Plane Enable			
Size	Document Number	Rev	
Enrico Caruso 14 MLK DIS		X02	
Date:	Tuesday, January 03, 2012	Sheet	36 of 104

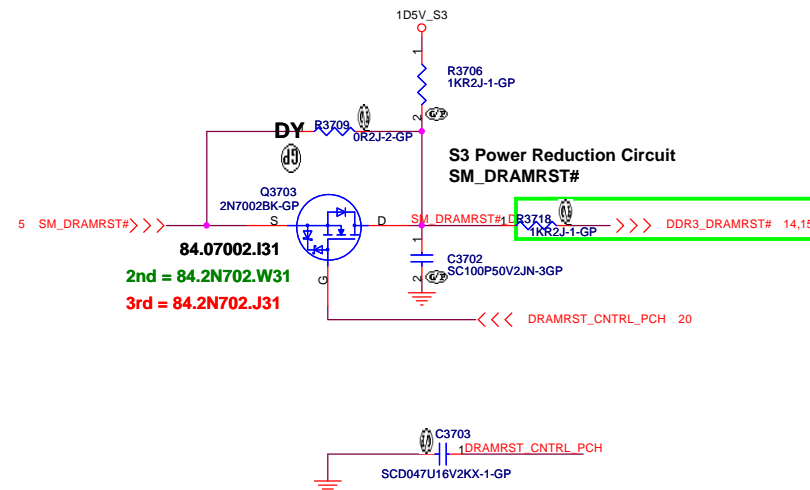
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



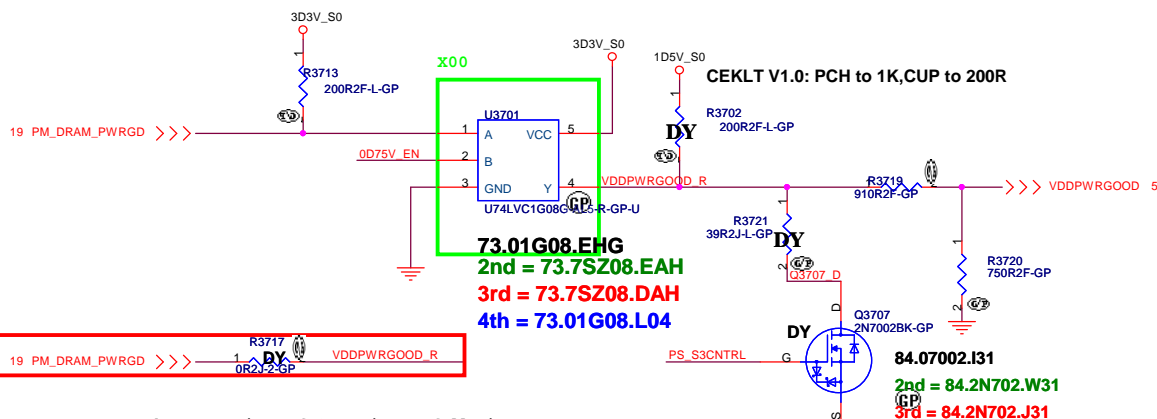
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55 f 200mV and the edge must be monotonic

<Variant Name>

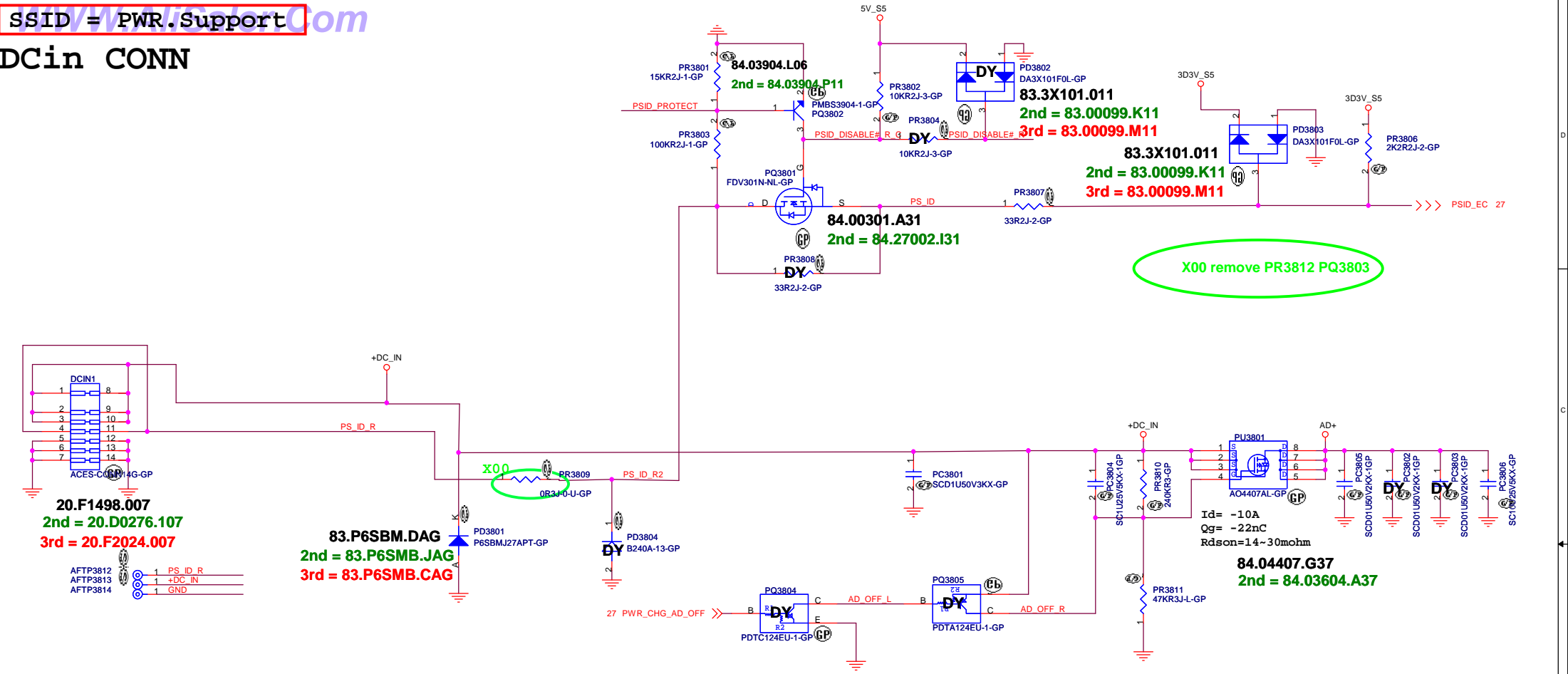
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **S3 Reduction Circuit**

Size: A3 Document Number: **Enrico Caruso 14 MLK DIS** Rev: **X02**

Date: Tuesday, January 03, 2012 Sheet 37 of 104

DCin CONN



X00 remove PR3812 PQ3803

<Variant Name>

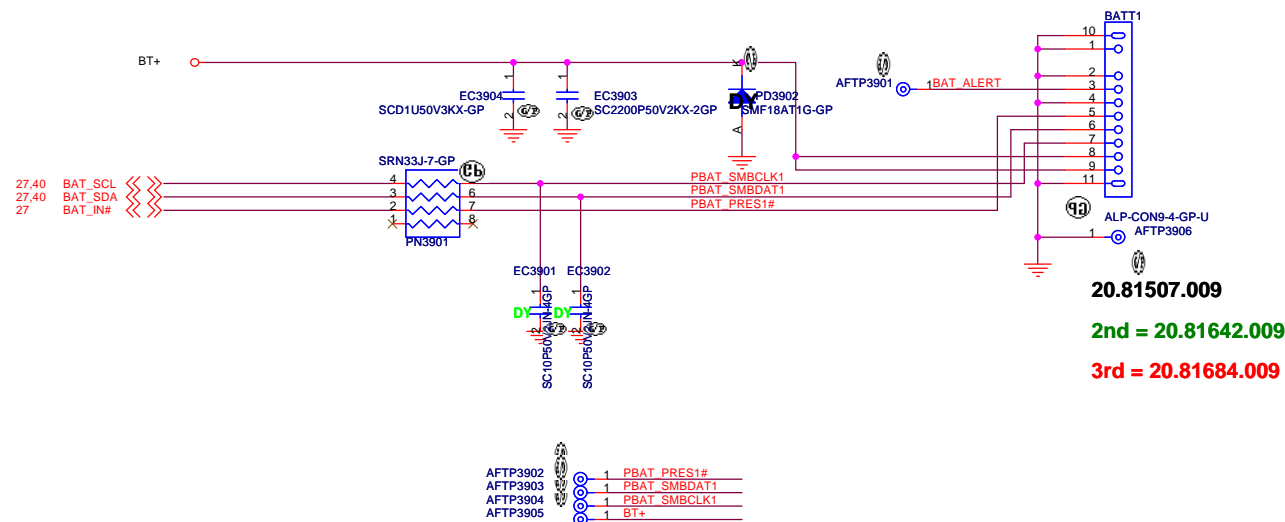
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **DCIN Jack**

Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X01
------------	--	-------------------

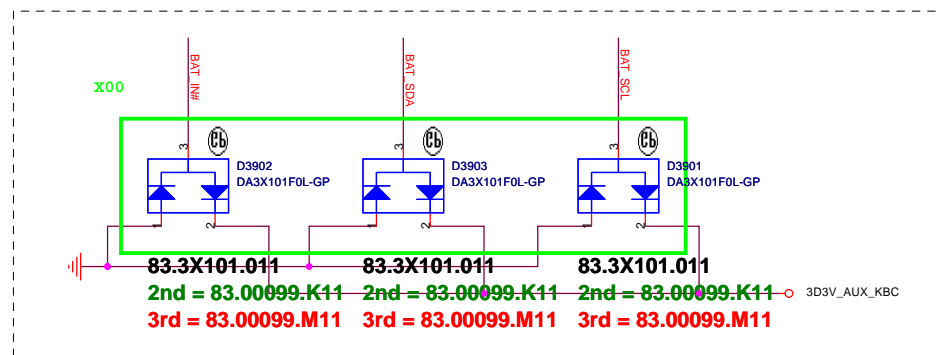
Date: Tuesday, January 03, 2012 Sheet 38 of 104

Batt Connector



For actual location, need to be swap all pin

Placement: Close to Batt Connector

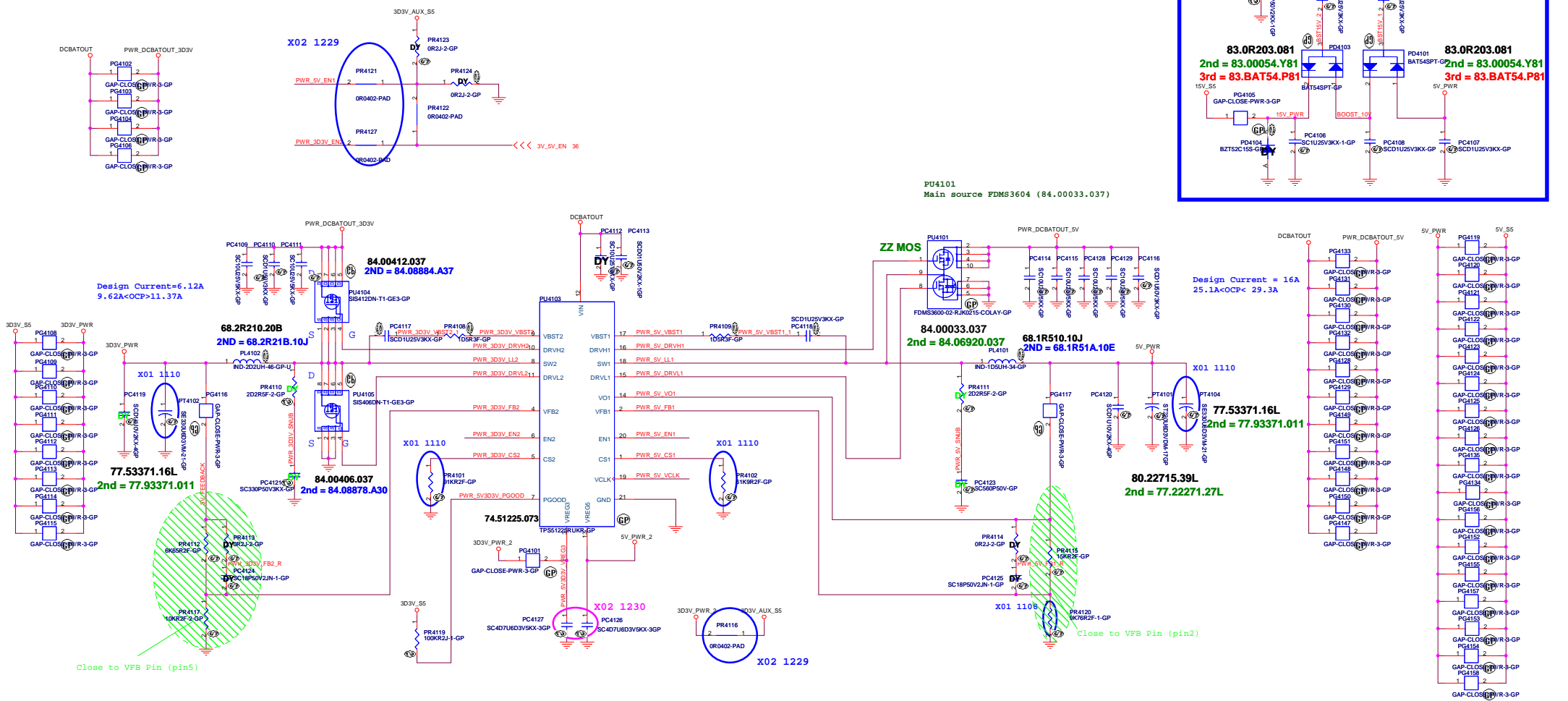


<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BATT CONN			
Size	Document Number	Rev	
A3	Enrico Caruso 14 MLK DIS	X01	
Date:	Tuesday, January 03, 2012	Sheet 39	of 104



SSID = PWR.Plane.Regulator 5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U6.3V M6.3*5.7 15mOhm / 77.53371.04L
H/S: SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S: SI7716ADN-T1-GE3 / 13.5mohm/16.5mohm@4.5Vgs / 84.07716.037

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 220U 6.3V PS1V01227M 25mohm 2.236Arms NEC TOKIN/77.C2271.00L
O/P cap: CHIP CAP POL 330U6.3V M6.3*5.7 15mOhm / 77.53371.04L
H/S,L/S: FDMS3604S / 7.5mohm/9.8mohm@4.5Vgs, 2.6mohm/3.2mohm@4.5Vgs/ 84.03604.037

<Variant Name>

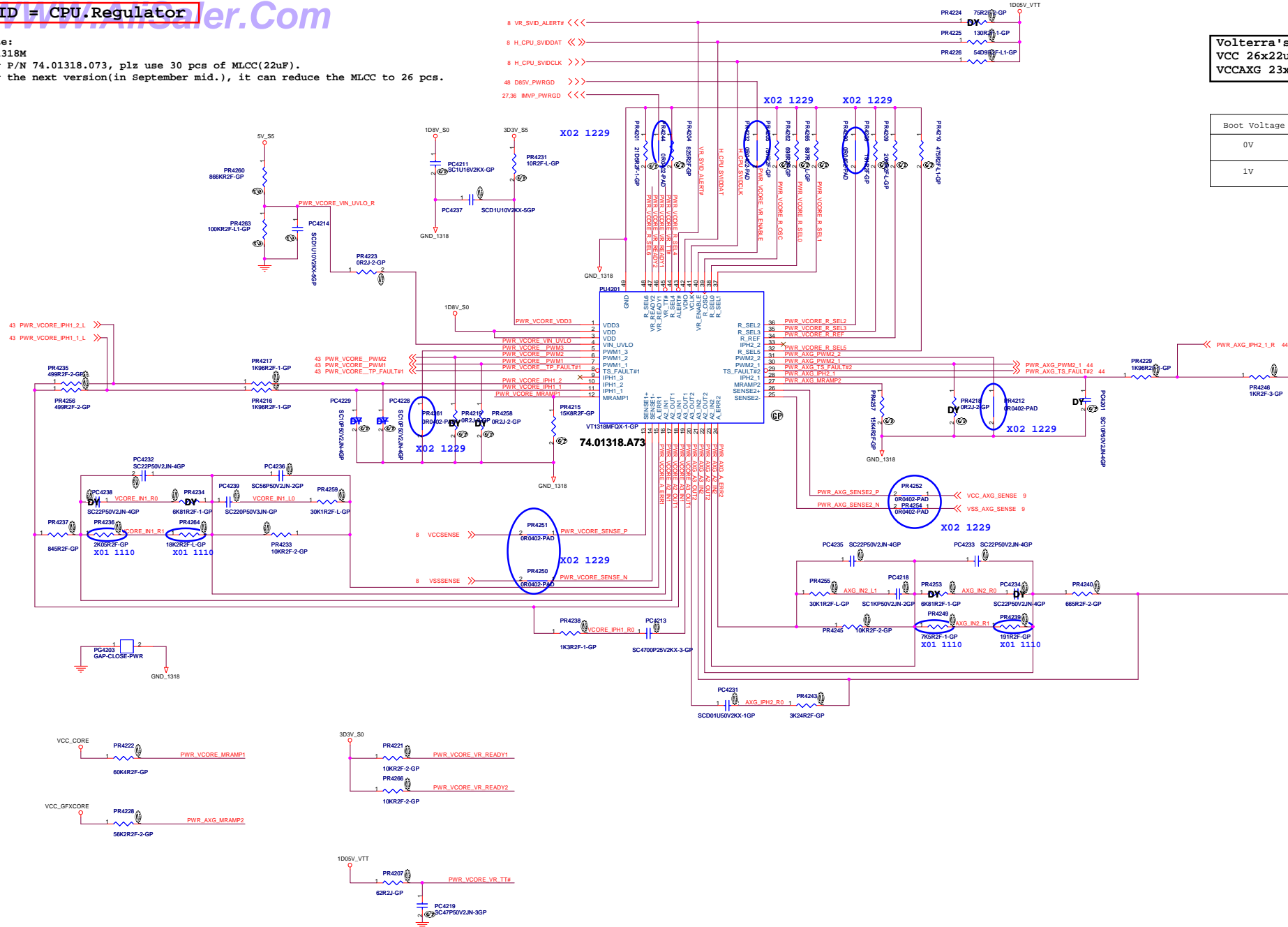
DELL Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 300, Taiwan, R.O.C.

Title			
3V/5V TPS51225			
Size	Document Number	Rev	
A2	Enrico Caruso 14 MLK DIS	X01	
Date:	Tuesday, January 03, 2012	Sheet	41 of 104

Note:
VT1318M
For P/N 74.01318.073, plz use 30 pcs of MLCC(22uF).
For the next version(in September mid.), it can reduce the MLCC to 26 pcs.

Volterra's suggestion: VCC 26x22uF for 2-PHASE VCC VCCAXG 23x22uF for 1-PHASE VCCAXG
--

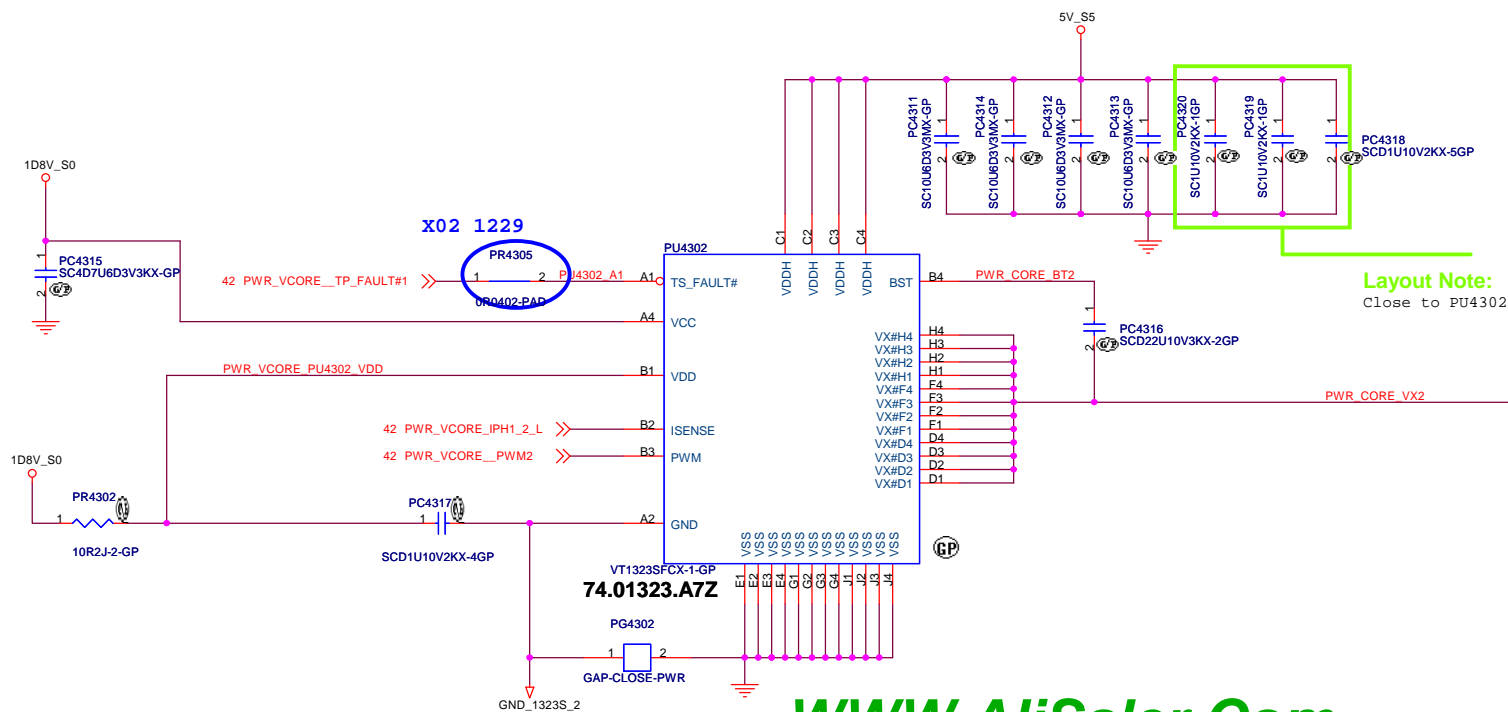
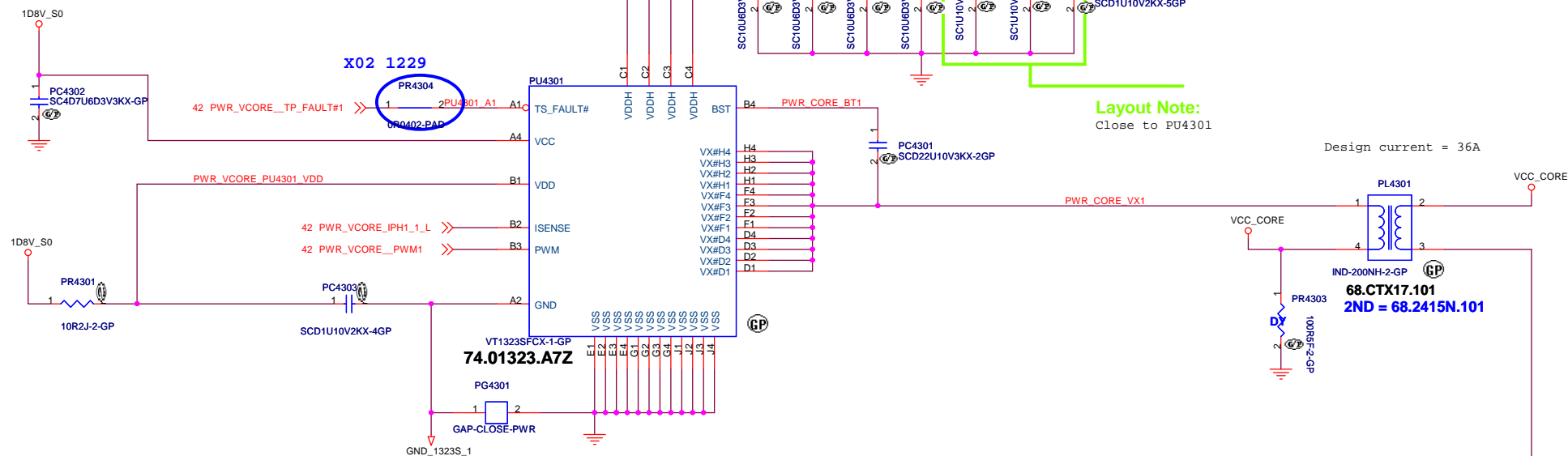
Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm



<Variant Name>

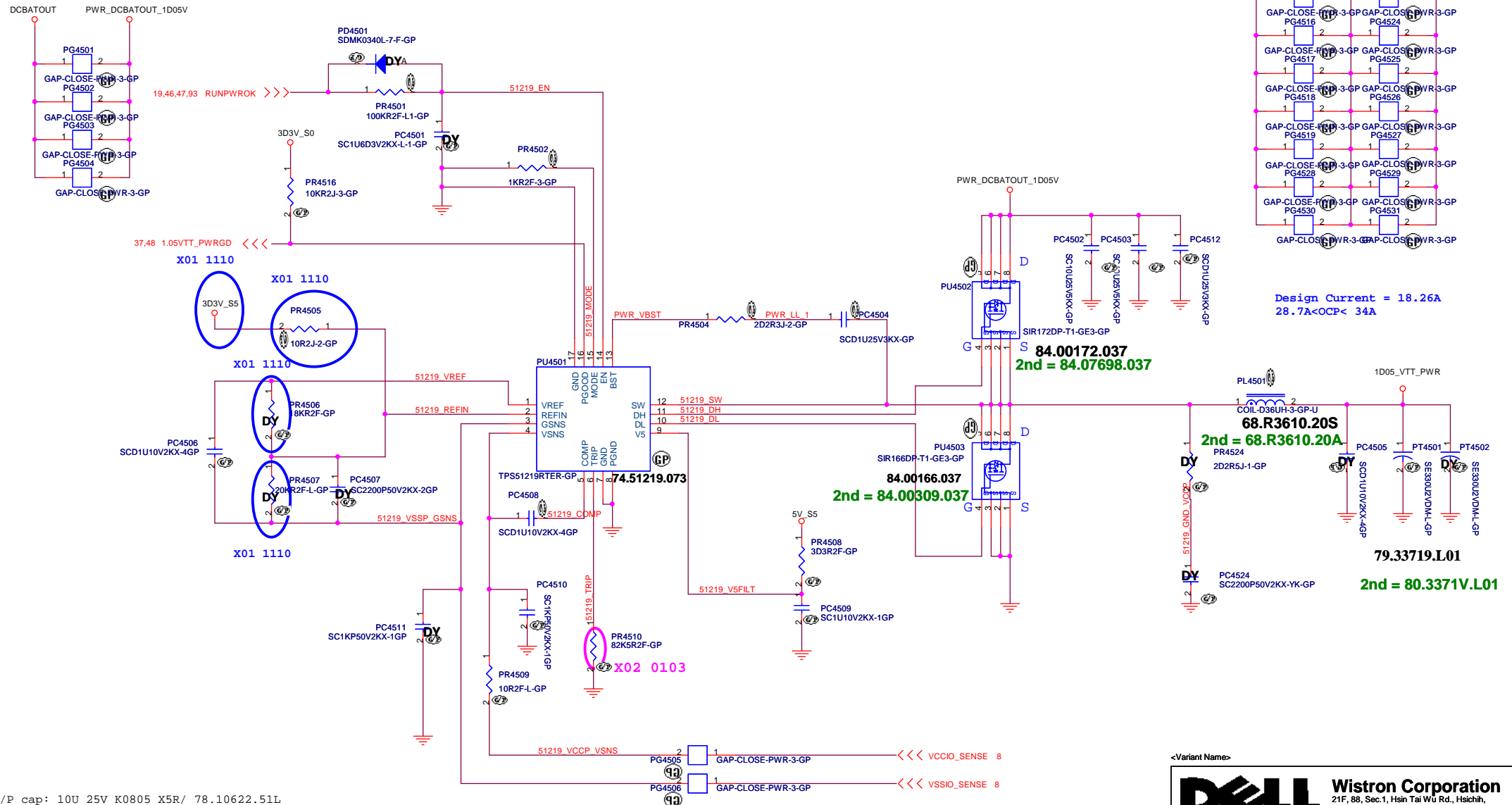
DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				VT1318 CPU CORE(1/3)			
Size	Document Number					Rev	
A2	Enrico Caruso 14 MLK DIS					X01	
Date:	Tuesday, January 03, 2012	Sheet	42	of	104		

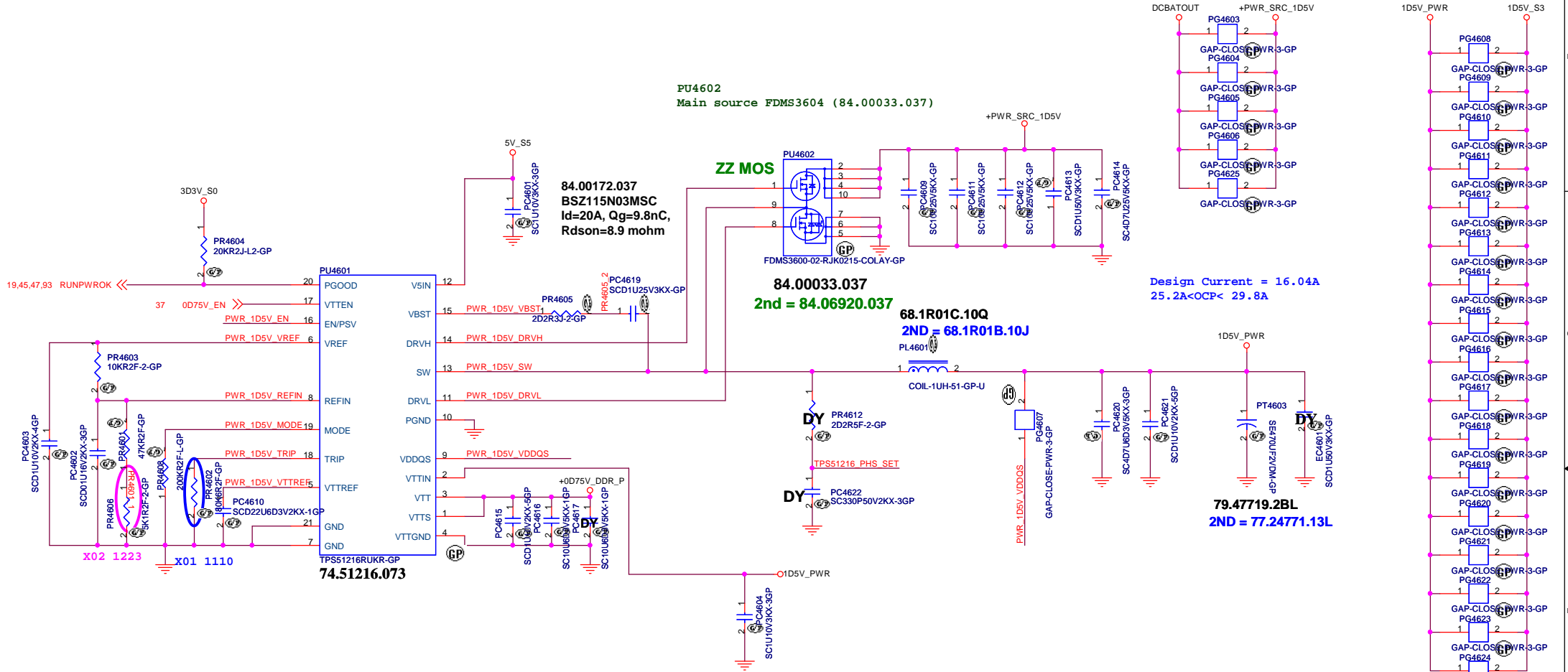




TPS51219 for 1D05V_PCH/VCCP_CPU



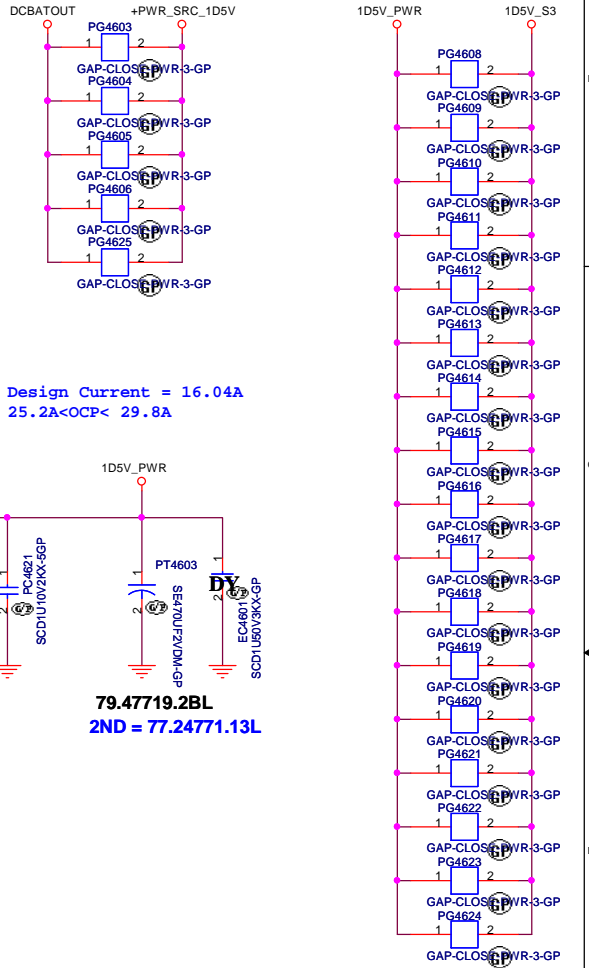
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10UJ
O/P cap: 330U2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SIR166DP / 0.32mohm/0.4mOhm@4.5Vgs/ 84.00166.037



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M Cynotec 3mohm/3.3mohm Isat =28Arms68.1R01C.10Q
O/P cap: CHIP CAP 470UF 2V EEFSX0D471X 6mOhm 3.5Arm/Panasonic/79.47719.2BL
H/S,L/S: FDMS3604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

TPS51216 +1.5V SUS

Size

Document Number

Rev

A3

Enrico Caruso 14 MLK DIS

X01

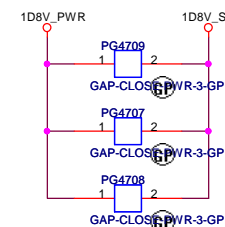
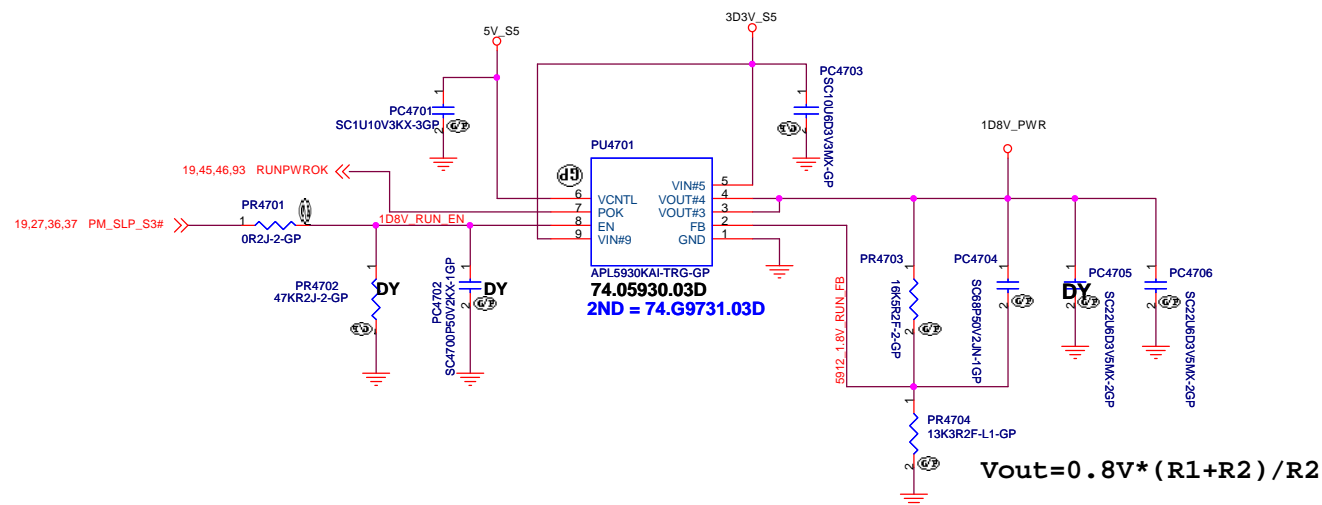
Date: Tuesday, January 03, 2012

Sheet 46 of 104

SSID = PWR.Plane.Regulator_1p8v

APL5930 for 1D8V_S0

+1.8V_RUN
Design current = 1.086A



<Variant Name>

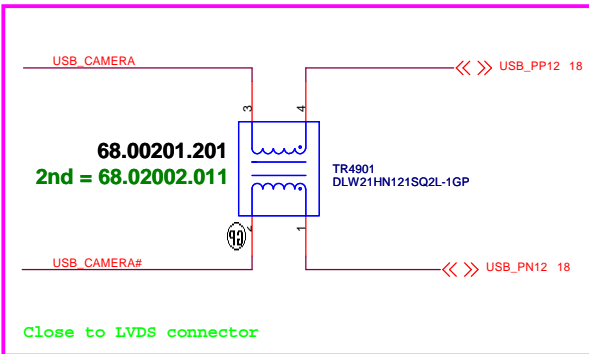
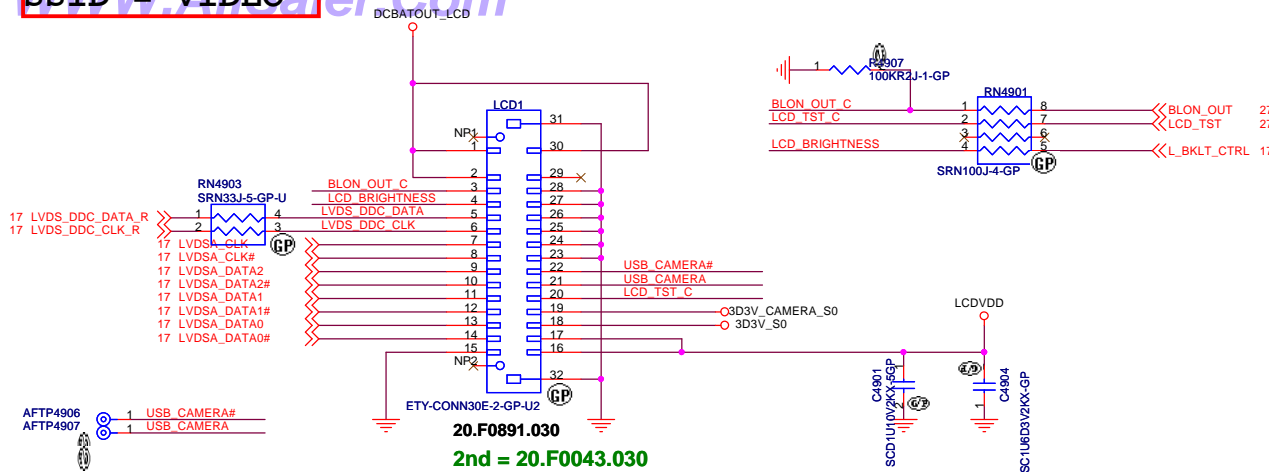
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title APL5930 1D8V S0			
Size A3	Document Number Enrico Caruso 14 MLK DIS		Rev X01
Date: Tuesday, January 03, 2012		Sheet 47	of 104

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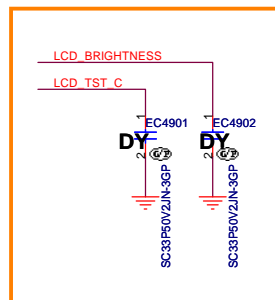
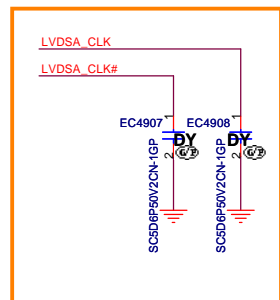
I_{max}=6A
OCP>9A
VCCSA=0.9V

SSID = VIDEO



X02 0103
remove R4903,R4904 co-lay position

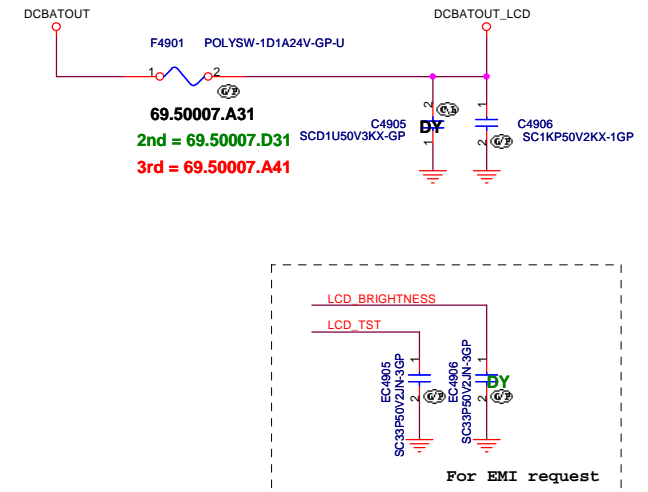
Close to LVDS connector



For EMI request

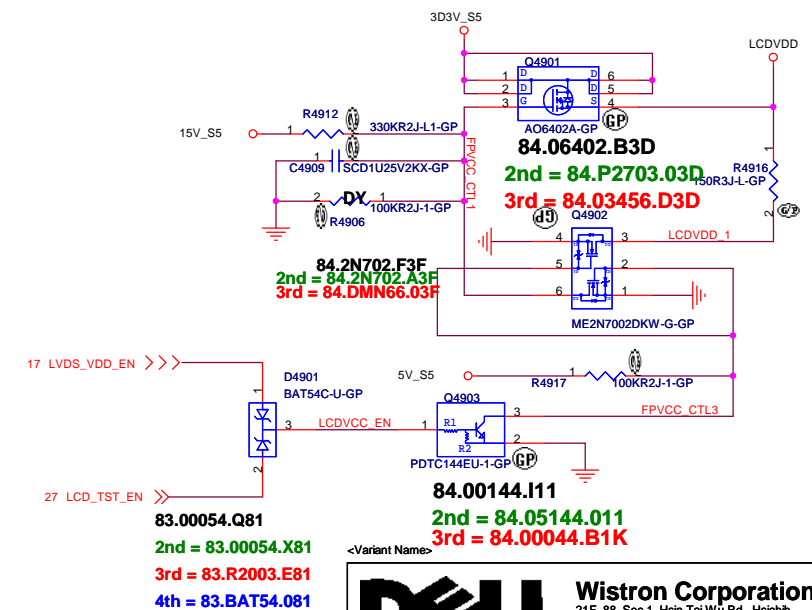
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER

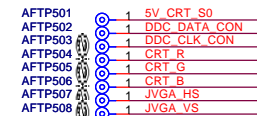
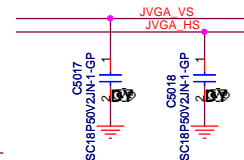
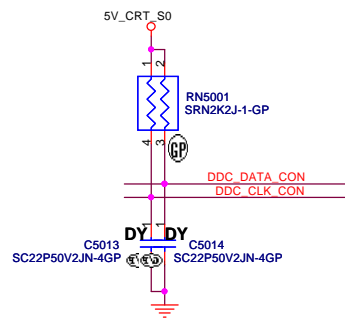
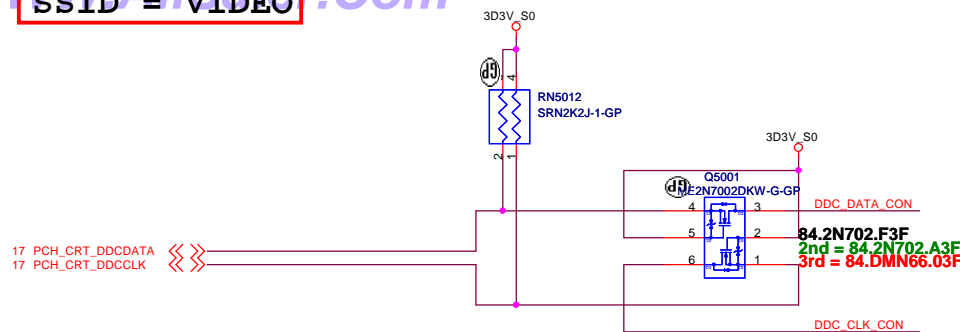


DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

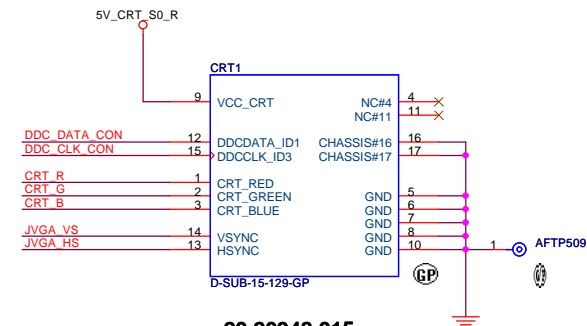
LCD Connector			
Size	Document Number	Rev	
A3	Enrico Caruso 14 MLK DIS	X02	
Date:	Tuesday, January 03, 2012	Sheet	49 of 104

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SSID = VIDEO



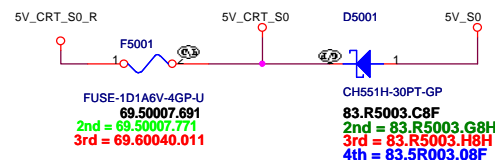
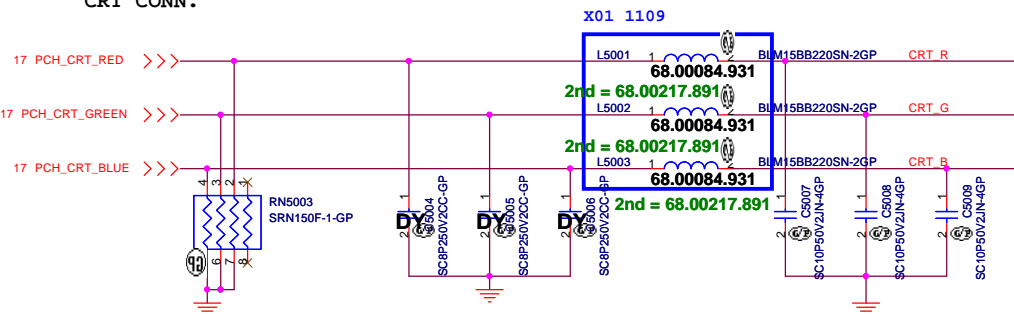
11/29 change CRT1 to 20.20927.015



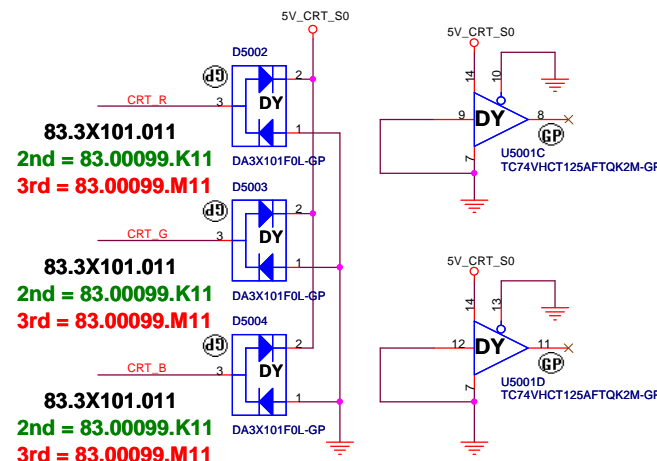
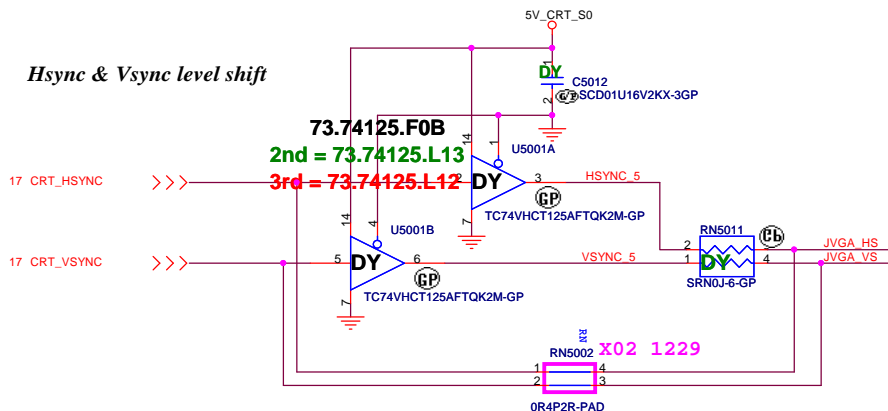
20.20948.015
2nd = 20.20945.015

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift



CLOSE TO TRANSFORMER

<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

File: **CRT Connector**

Size: A3 Document Number: **Enrico Caruso 14 MLK DIS** Rev: **X02**

Date: Tuesday, January 03, 2012 Sheet: 50 of 104

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

X02 1229

HDMI_CLK_R_C 1 R5101 2 HDMI_CLK_R_C_CON
0R0402-PAD

HDMI_CLK_R_C# 1 R5102 2 HDMI_CLK_R_C#_CON
0R0402-PAD

changed R5101,R5102 to short pad,
removed TR5101 CMC footprint

HDMI_DATA0_R_C 1 R5104 2 HDMI_DATA0_R_C_CON
0R0402-PAD

HDMI_DATA0_R_C# 1 R5103 2 HDMI_DATA0_R_C#_CON
0R0402-PAD

changed R5103,R5104 to short pad,
removed TR5102 CMC footprint

HDMI_DATA1_R_C 1 R5106 2 HDMI_DATA1_R_C_CON
0R0402-PAD

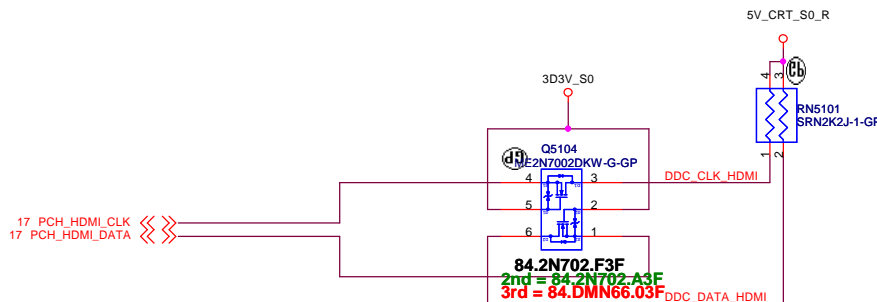
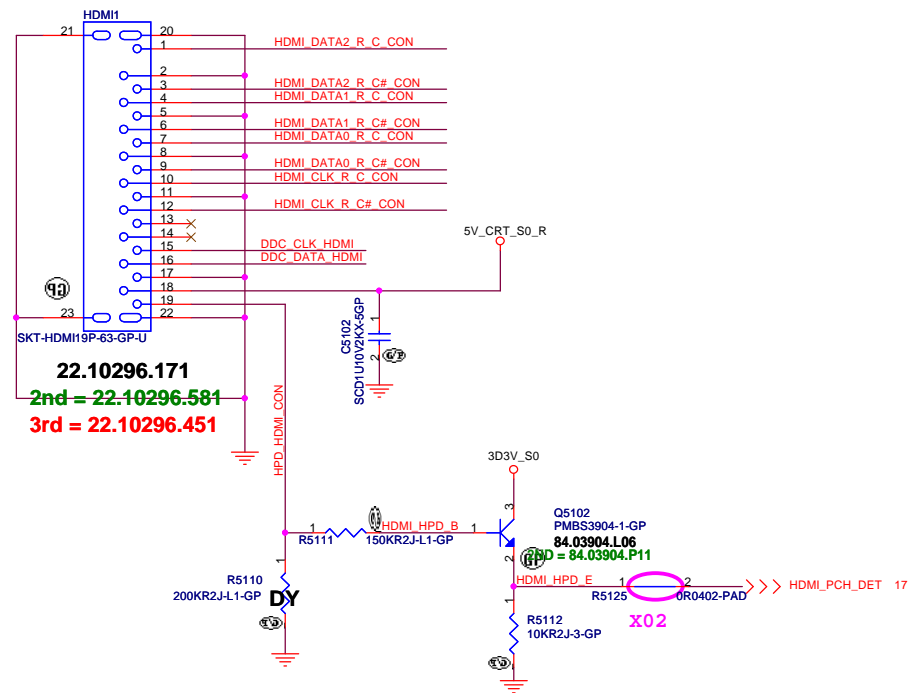
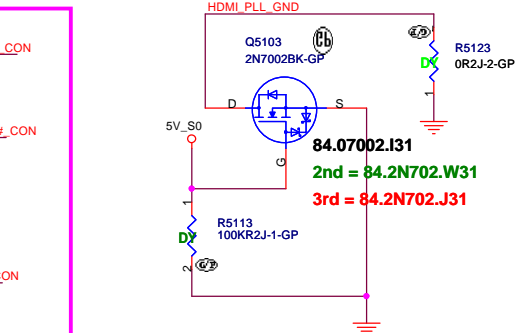
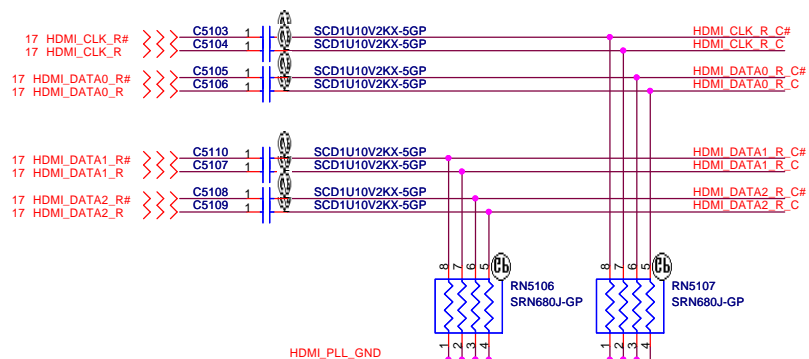
HDMI_DATA1_R_C# 1 R5105 2 HDMI_DATA1_R_C#_CON
0R0402-PAD

changed R5105,R5106 to short pad,
removed TR5103 CMC footprint

HDMI_DATA2_R_C 1 R5108 2 HDMI_DATA2_R_C_CON
0R0402-PAD

HDMI_DATA2_R_C# 1 R5107 2 HDMI_DATA2_R_C#_CON
0R0402-PAD

changed R5107,R5108 to short pad,
removed TR5104 CMC footprint



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

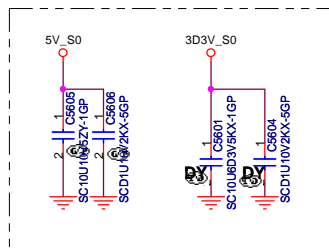
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<Variant Name>

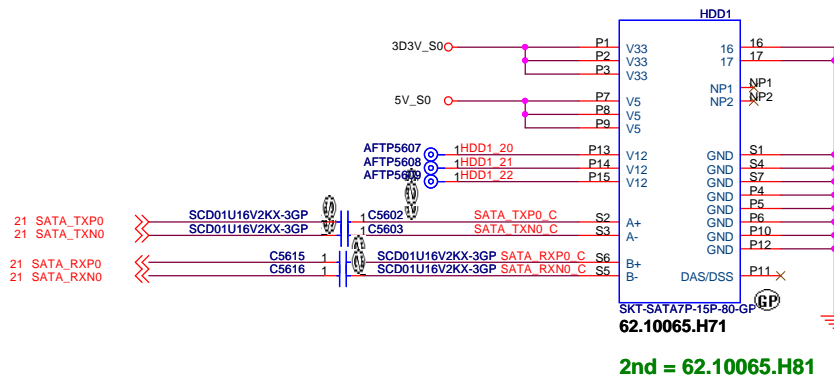
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: HDMI Level Shifter/Connector			
Size: A3	Document Number: Enrico Caruso 14 MLK DIS	Rev: X02	
Date: Tuesday, January 03, 2012	Sheet: 51	of 104	

SSID = SATA

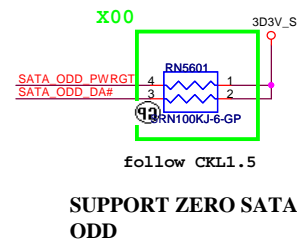
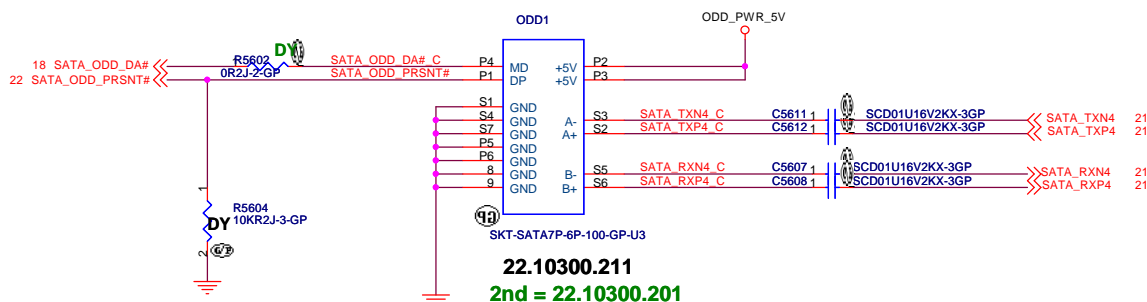
SATA HDD Connector



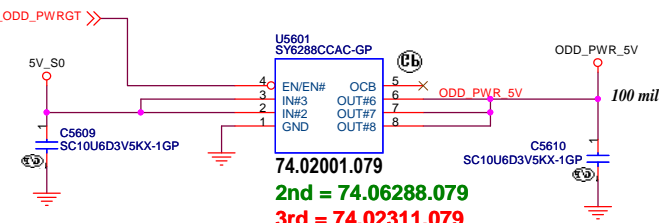
Close to HDD1



ODD Connector

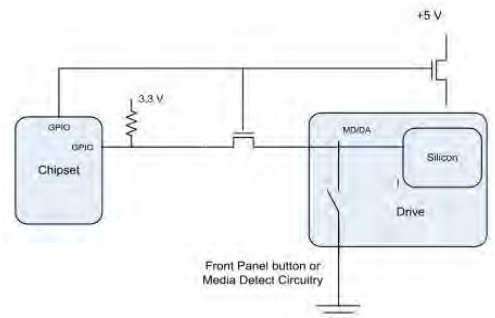
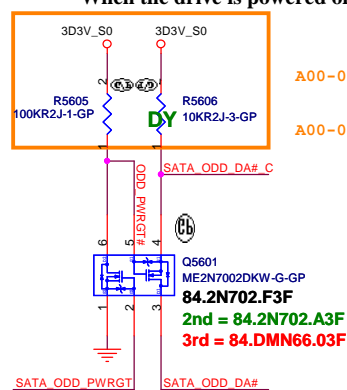


SATA Zero Power ODD



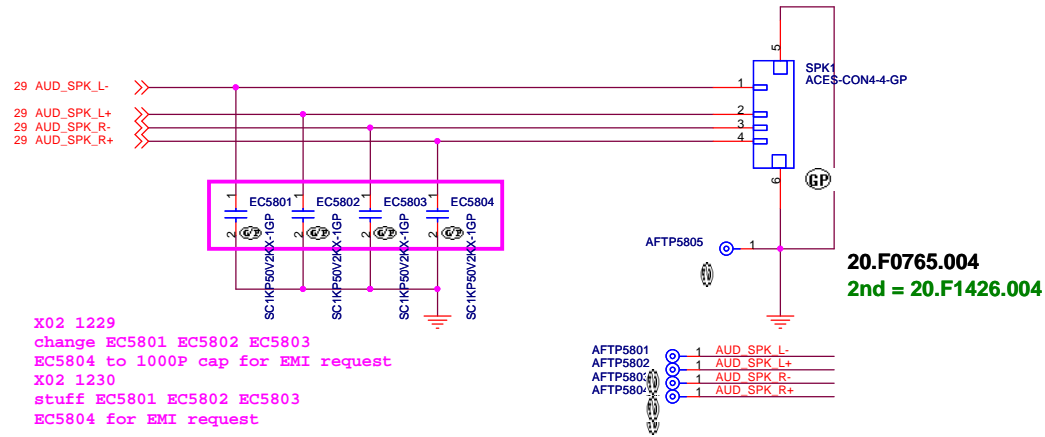
Current limit
Active High
typ => 2.5A

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

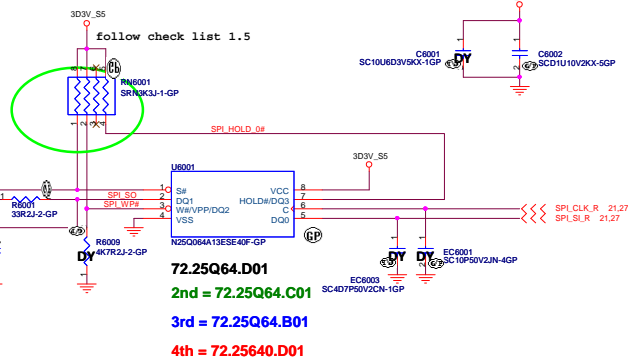


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Speaker Connector




```
SSID = Flash.ROM
```



3D3V_AUX_SS

RTC_AUX_SS

C6003
SC1U6D3V20K-GP

C6001

CH715FPT-4GP

83.R0304.B81

2nd = 83.R2094.C81

Width=20mils

RTC_PWR

RTC_VCC

R6006
100R2J-1-GP

RTC1

ACES-CON2-31-GP

20.F1606.002

2nd = 20.F1871.002

R6007 1

100R2J-2-GP

RTC_PWR

R6008
100R2J-1-GP

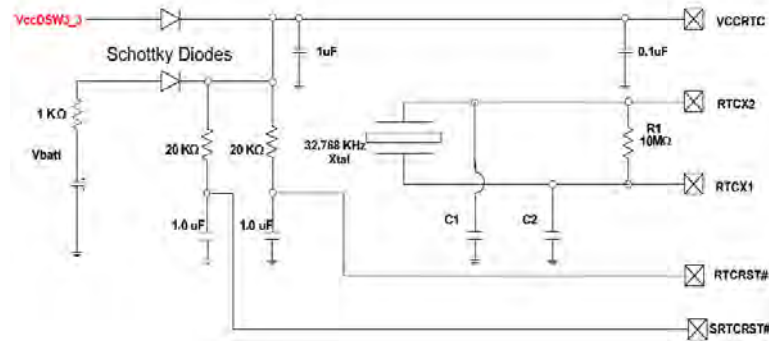
C6002
20V0020K-GP

84.07002.J31

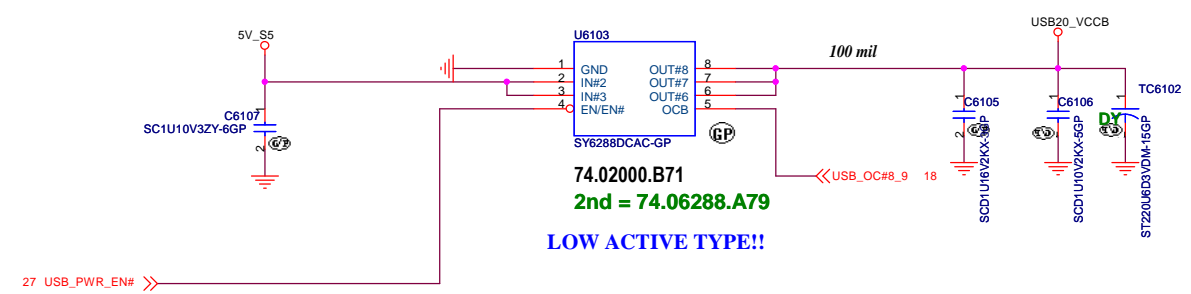
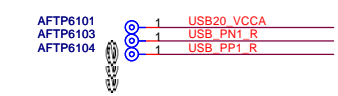
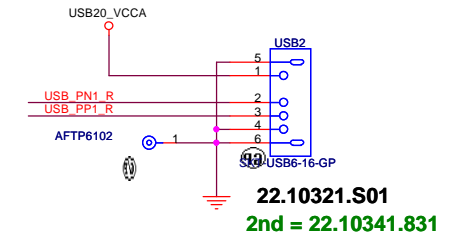
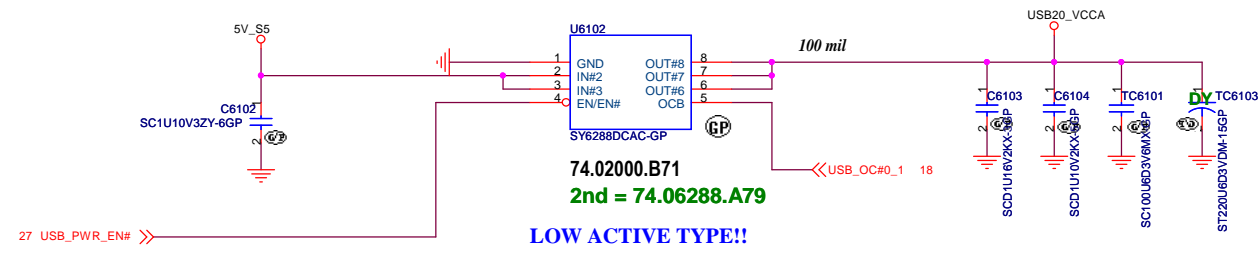
2nd = 84.2N702.W31

3rd = 84.2N702.J31

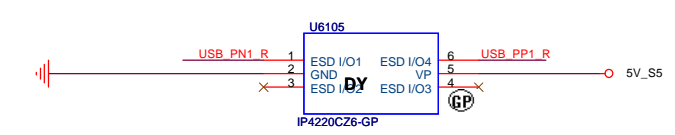
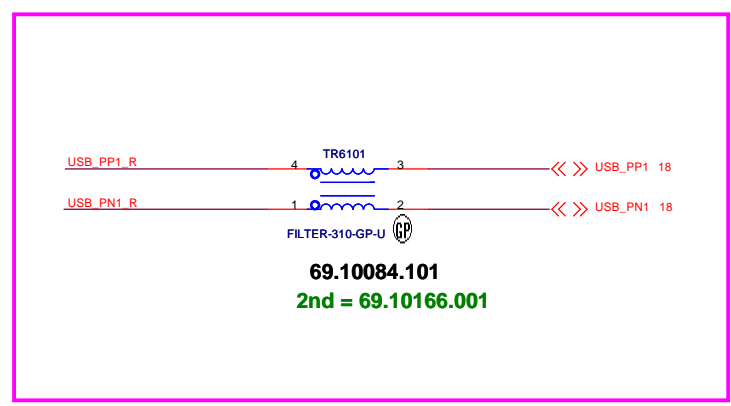
RTC_DET# 22



VccRTC is now connected to VccDSW3_3 through the Schottky diode instead of the 3.3V Sus well.

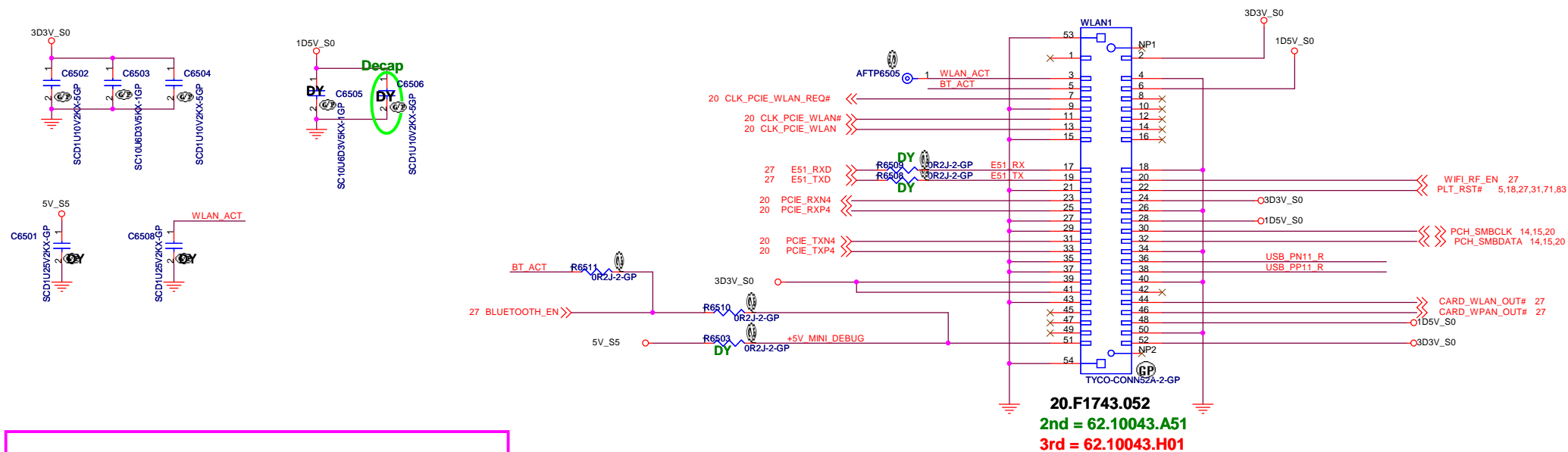


X02 1230
removed R6102,R6103 co-lay position



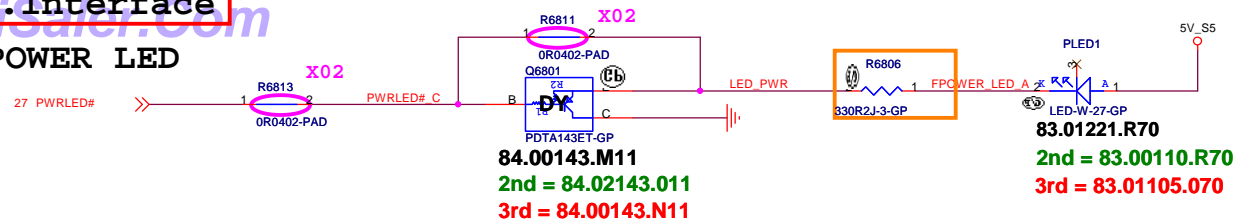
SSID = Wireless

Mini Card Connector(802.11a/b/g)

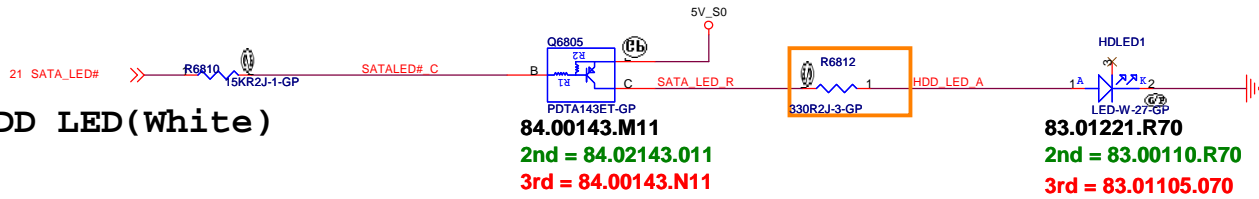


X02 1229
changed R6505,R6506 to short pad,
removed TR6501 CMC footprint

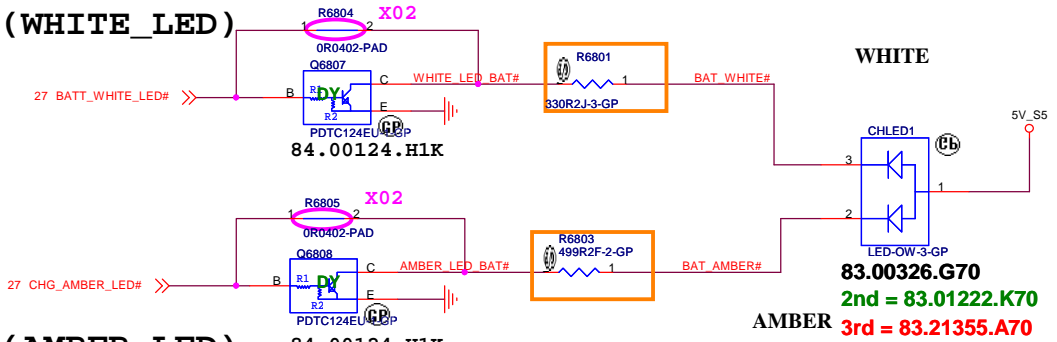
FRONT POWER LED



SATA HDD LED(White)

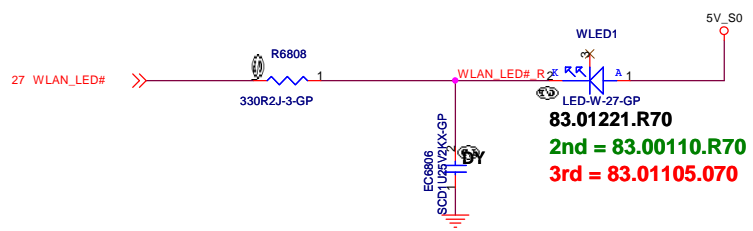


Battery LED2(WHITE_LED)



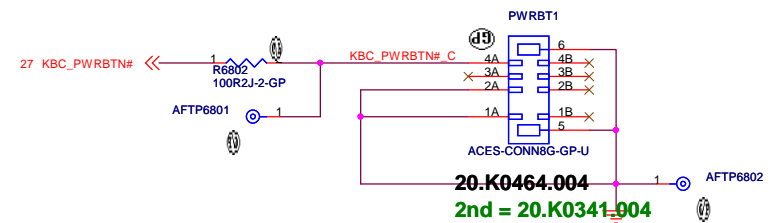
Battery LED1(AMBER_LED)

Wireless LED

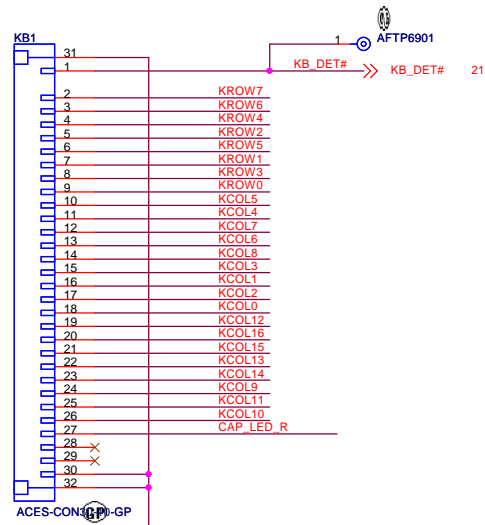


Place EC6806 near LED2

Power button



SSID = KBC



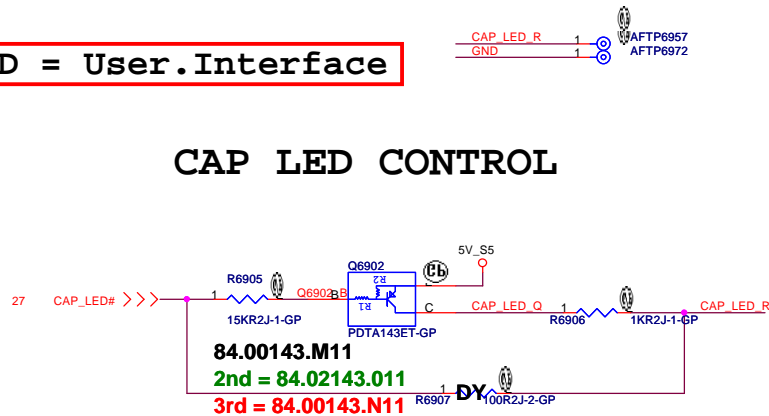
20.K0592.030

2nd = 20.K0621.030

3rd = 20.K0565.030

SSID = User.Interface

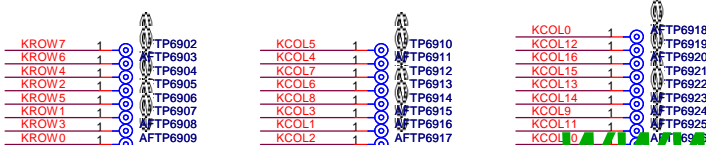
CAP LED CONTROL



84.00143.M11

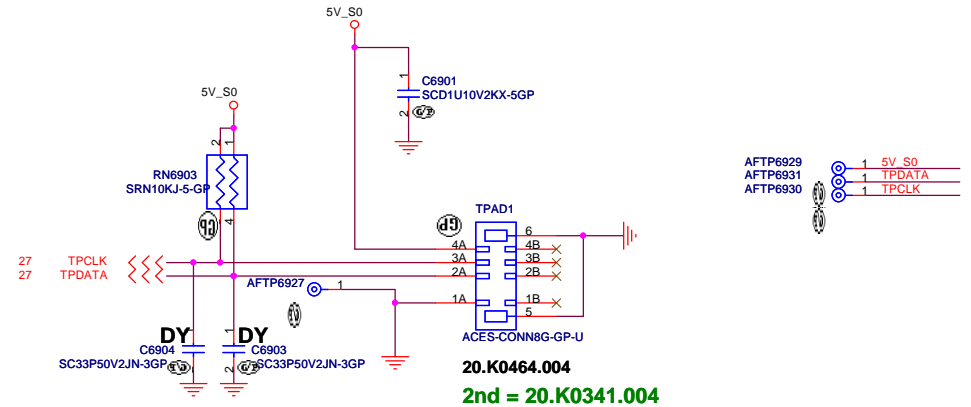
2nd = 84.02143.011

3rd = 84.00143.N11



SSID = Touch.Pad

TouchPad Connector



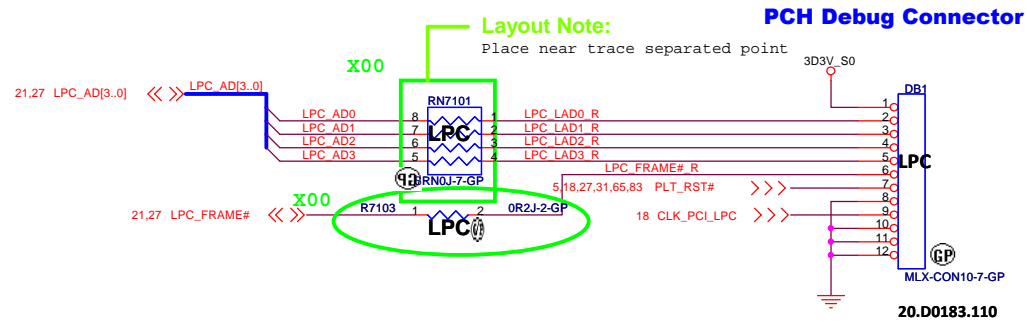
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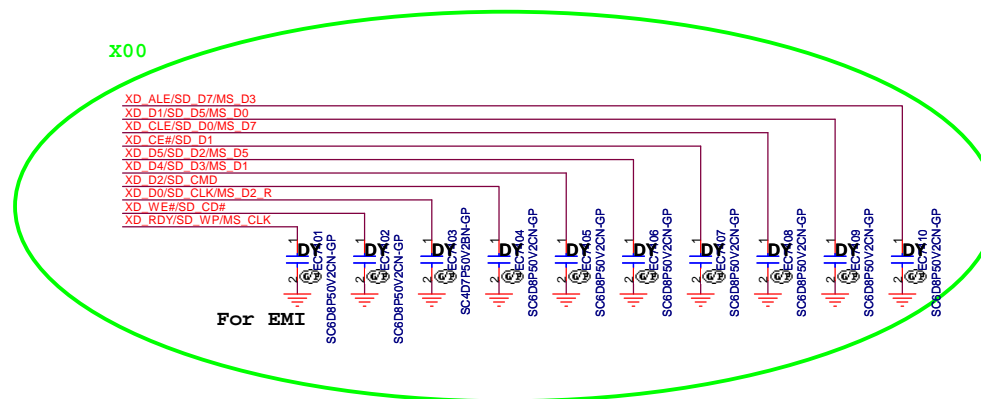
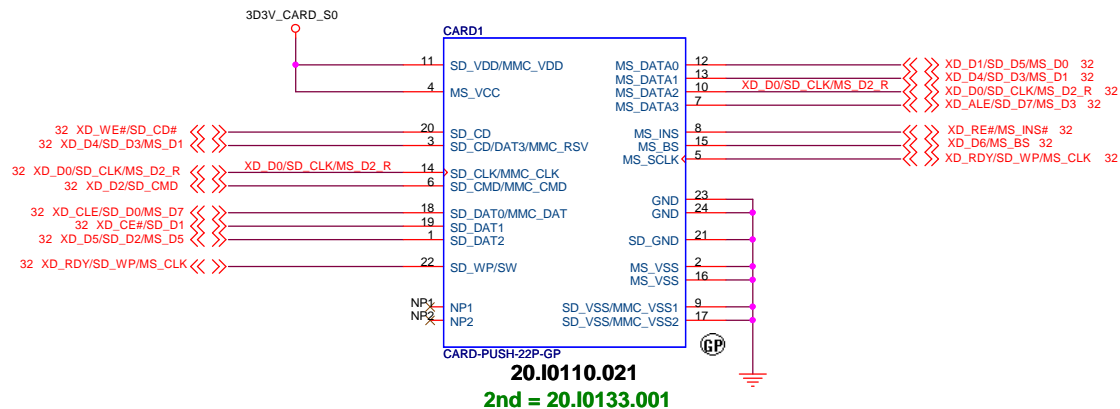
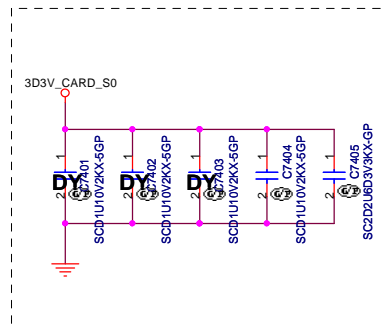
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<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

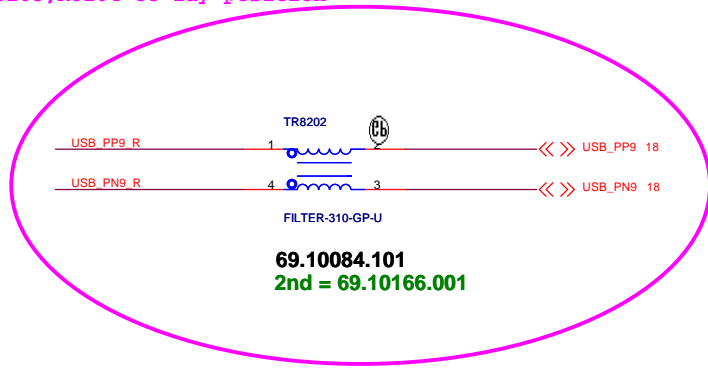
Key Board/Touch Pad		
Size A3	Document Number	Rev
Date: Tuesday, January 03, 2012	Enrico Caruso 14 MLK DIS	X02
Sheet 69	of 104	



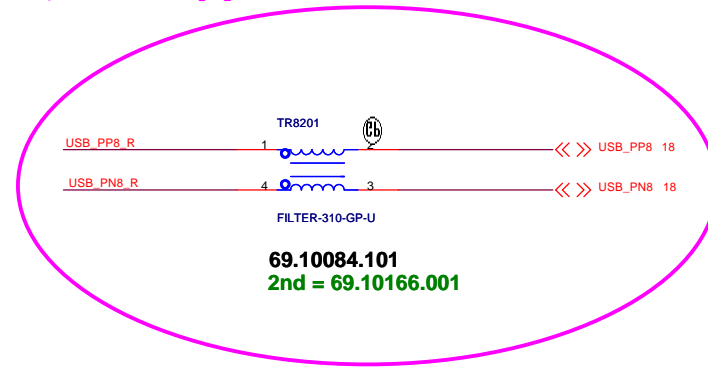


SSID = USB

X02 1230
removed R8203,R8204 co-lay position

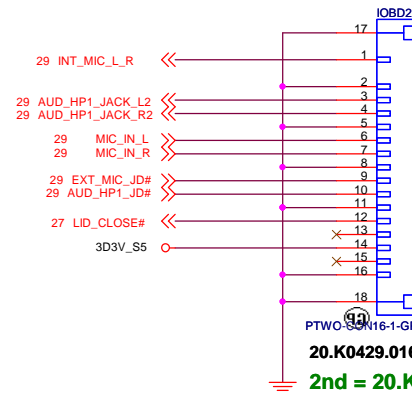
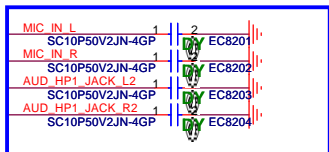


X02 1230
removed R8201,R8202 co-lay position

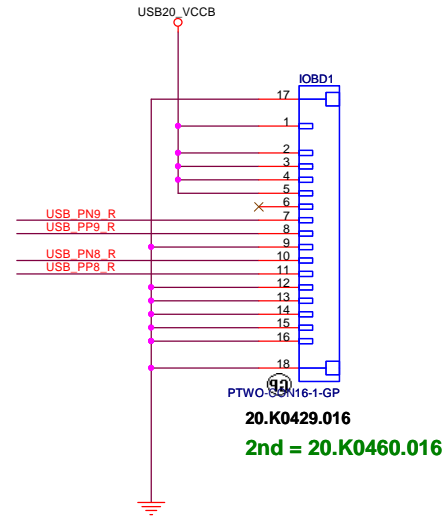


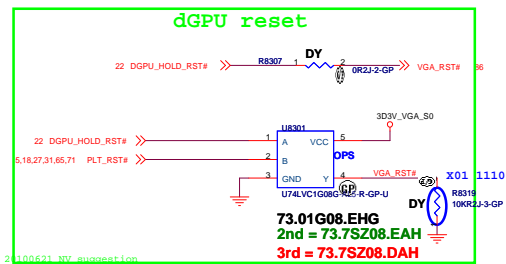
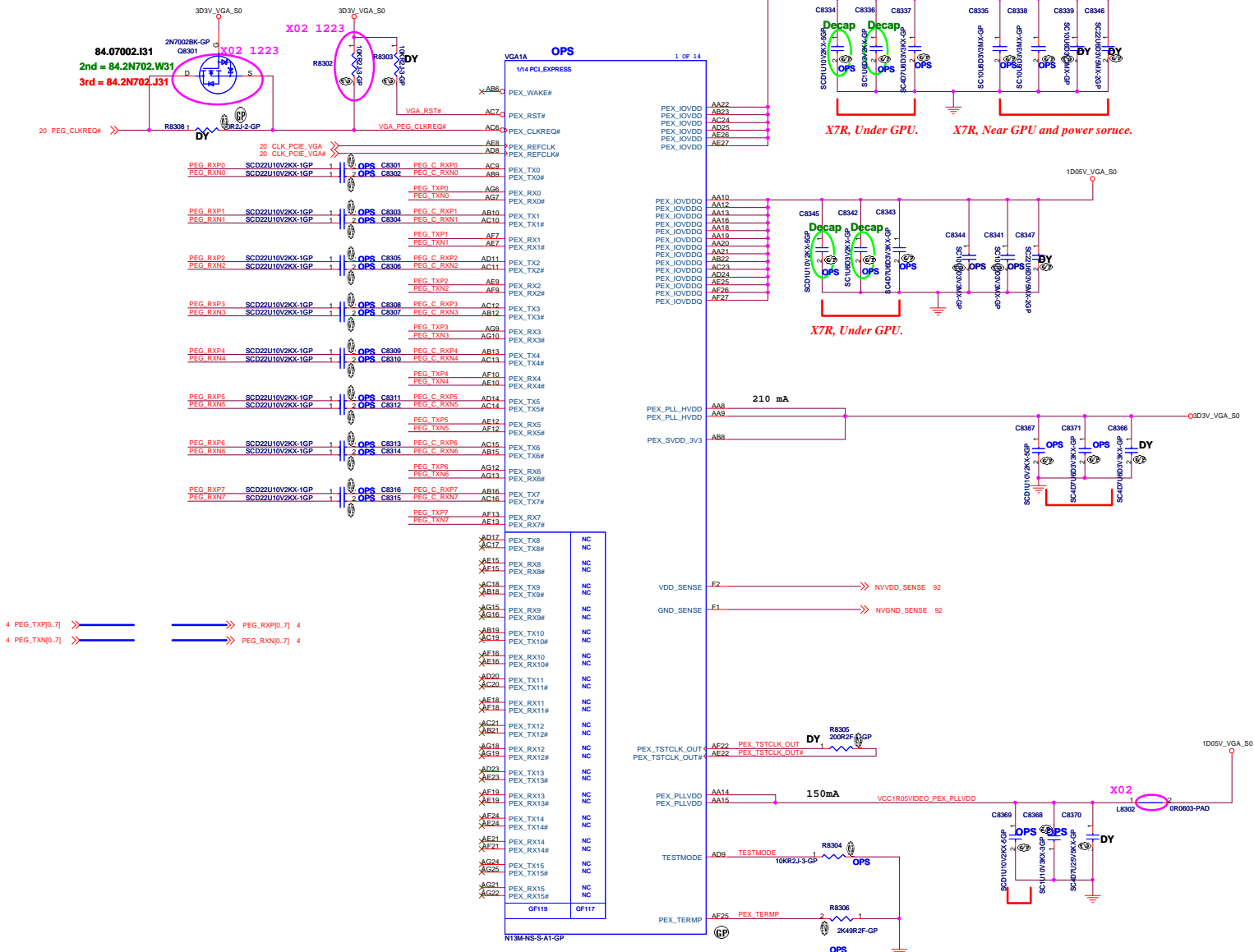
SSID = Audio

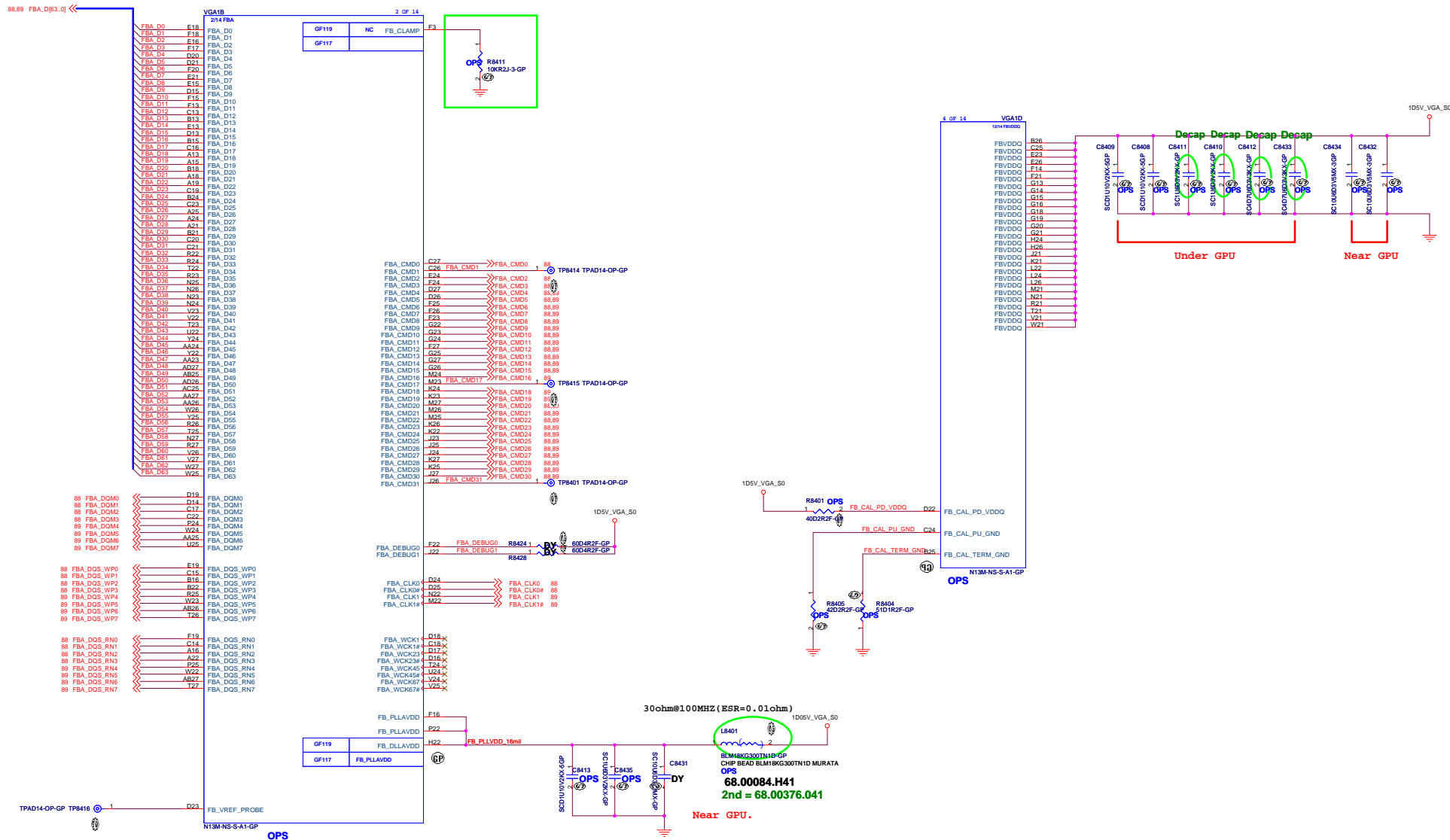
IOBD2 is for Audio board



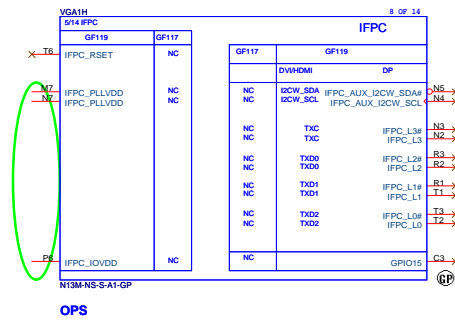
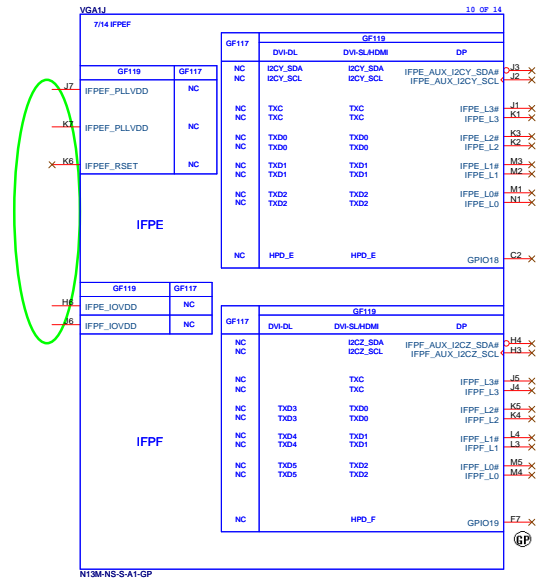
IOBD1 is for USB board



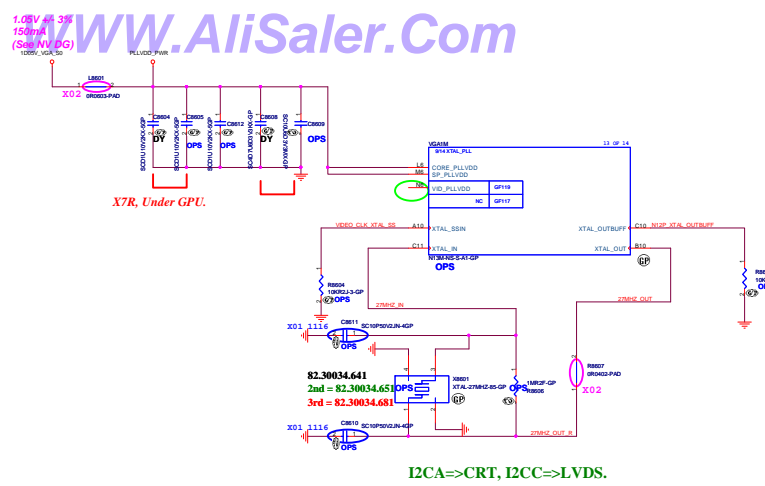




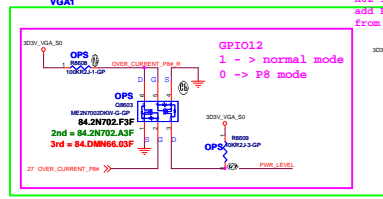
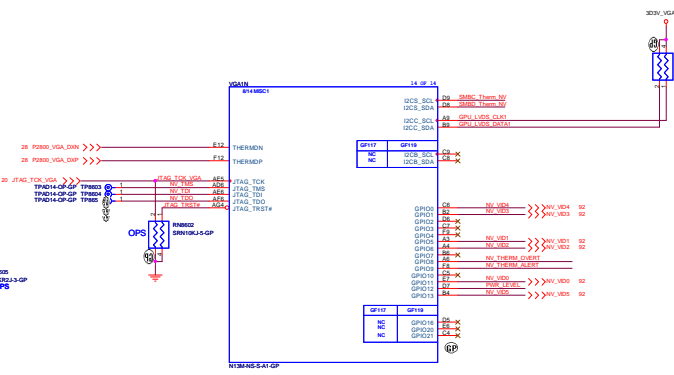
OPS



1.0V @ 3%
150mV
(See NV DG)
100V_VGA_S0



I2CA=>CRT, I2CC=>LVDS.

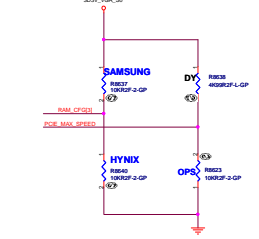
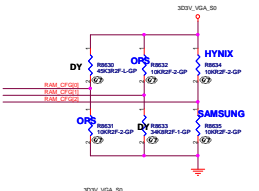
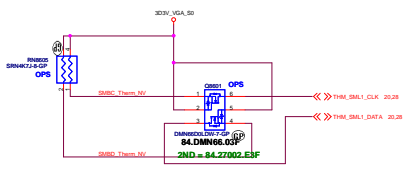


X02 1210
add R8508,Q8503;change Q8503.2 to OVER CURRENT_P8
from AC_PRESENT for OC trigger IPCC fuction

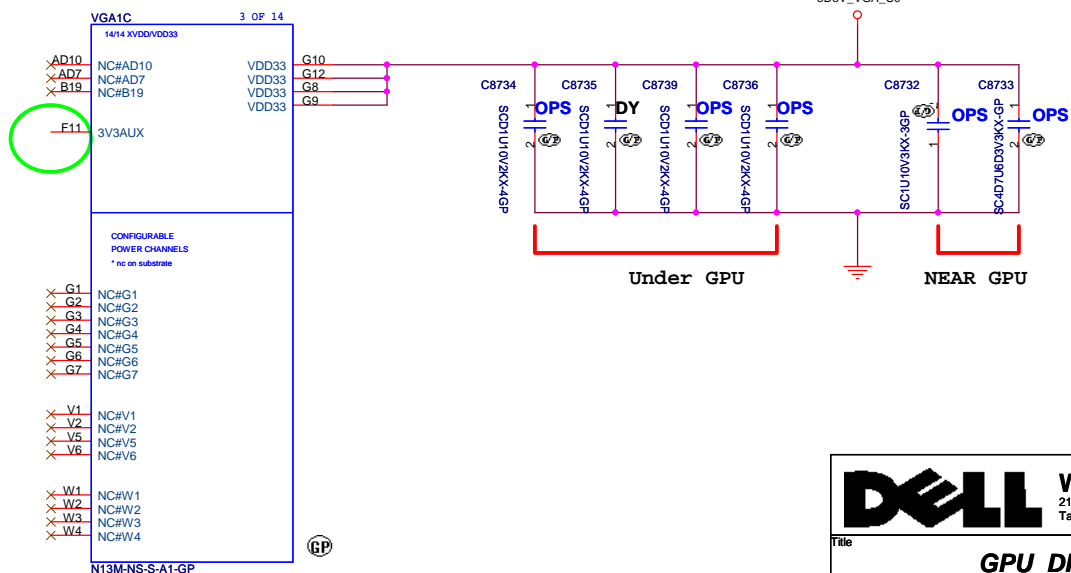
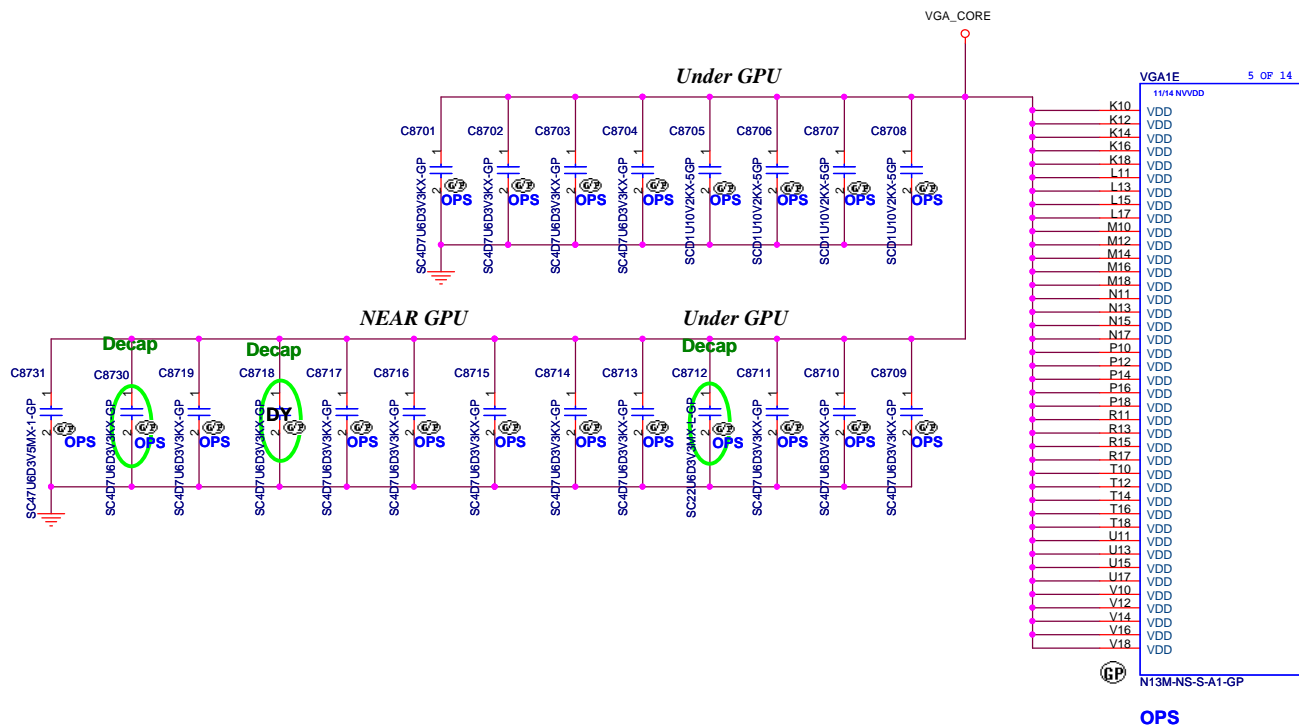
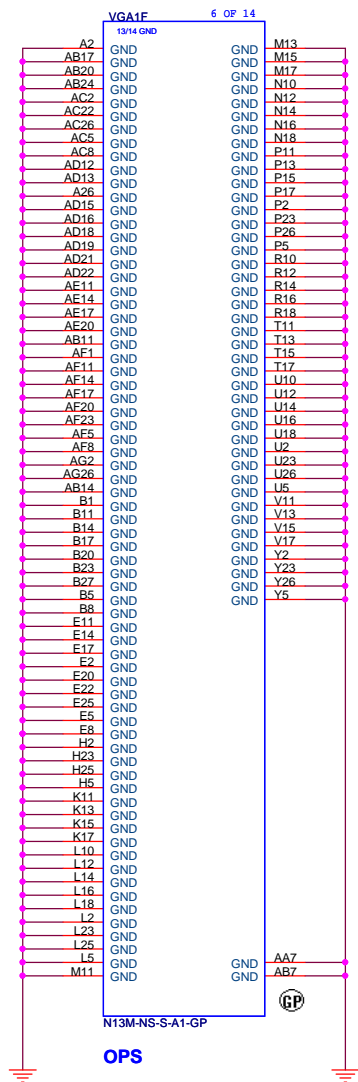


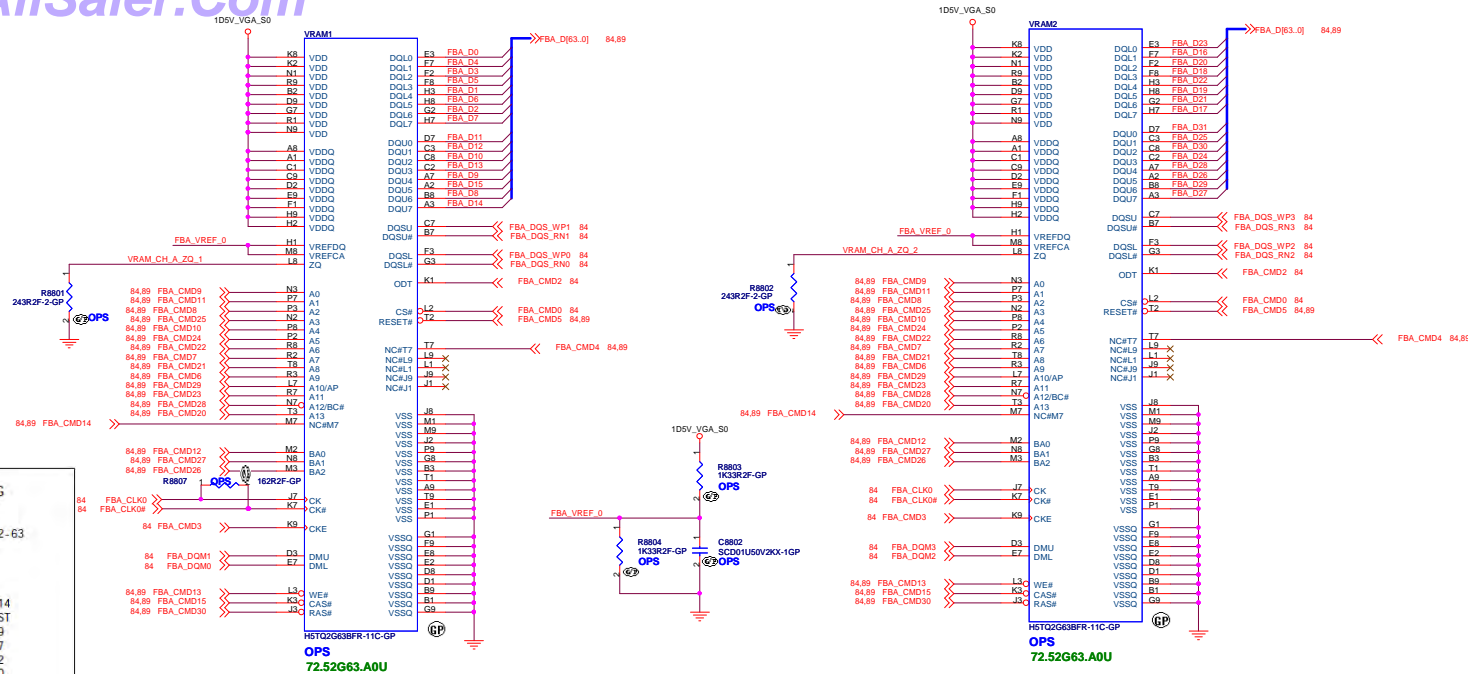
Hynix:72.52G63.A0U (HT31PSAA)
Samsung:72.42164.D0U (J1P0F2SAA)

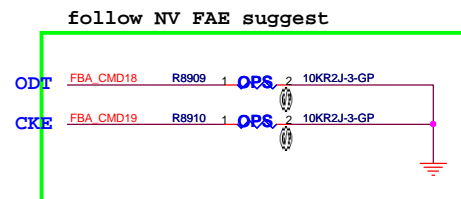
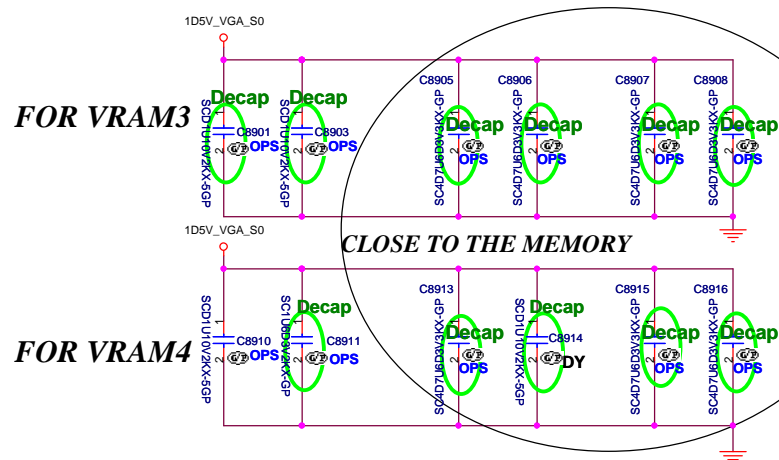
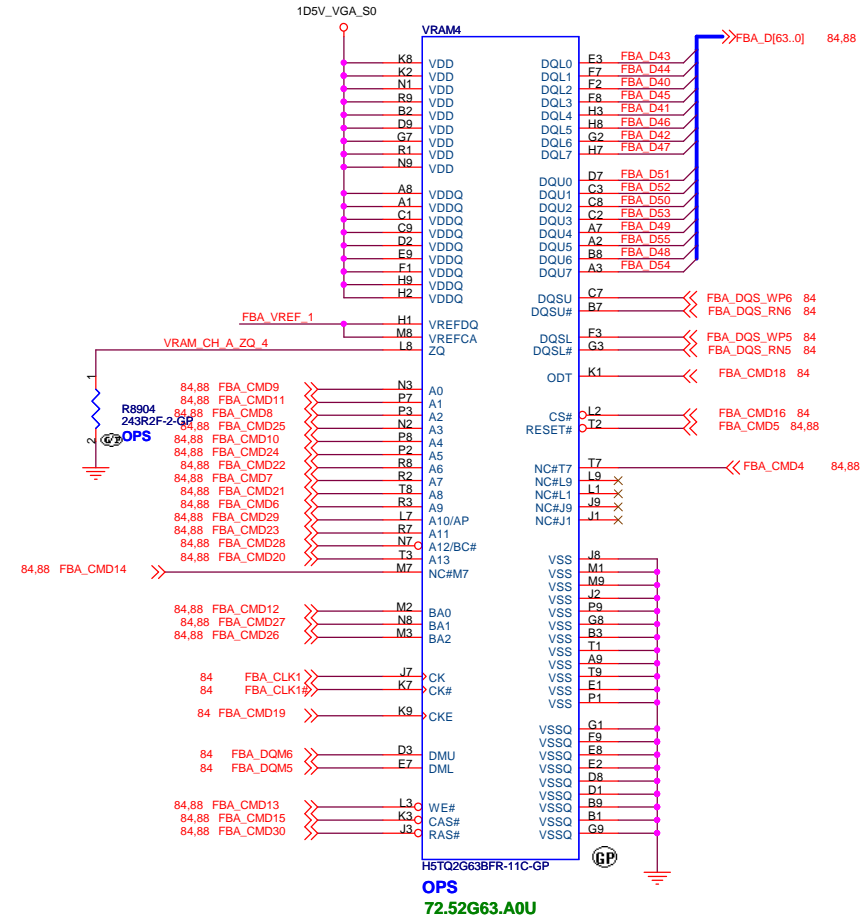
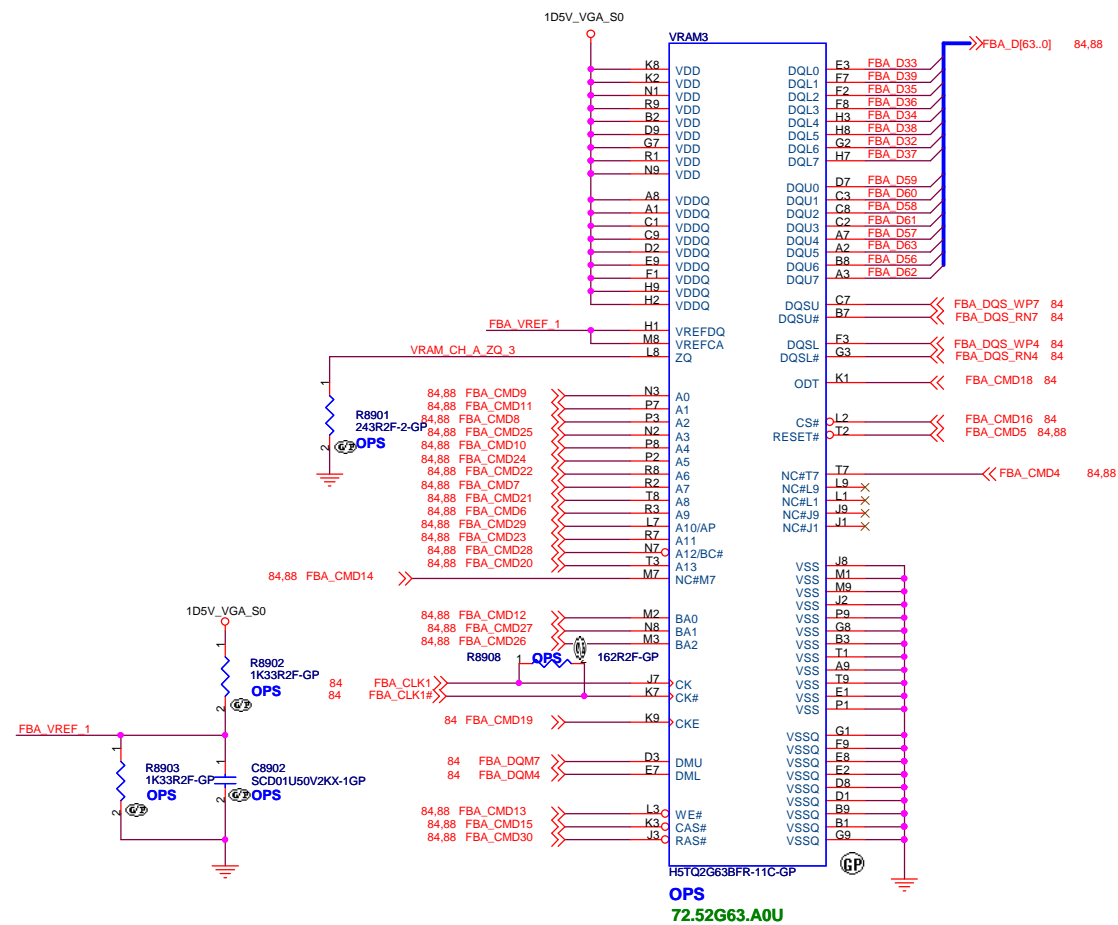
Strap Pin Name	Strap Mapping	Reset state	Polarity(Samsung B-S)	Polarity(Hynix E)
ROM_SCLK	SMB_ALT_ADDR0	10K ohm	pull down to GND	pull down to GND
ROM_S0	SMB_VEND0R	10K ohm	pull down to GND if no VBIOS ROM	pull down to GND if no VBIOS ROM
ROM_S0	VGA_DRV_E	10K ohm	pull down to GND (no display)	pull down to GND (no display)
STRAP0	RAM_CFG00	10K ohm	pull down to GND	pull down to GND
STRAP1	RAM_CFG01	10K ohm	pull up to 3.3V	pull up to 3.3V
STRAP2	RAM_CFG02	10K ohm	pull down to GND	pull down to GND
STRAP3	RAM_CFG03	10K ohm	pull down to GND	pull down to GND
STRAP4	PCI_MAX_SPEED	10K ohm	pull down to GND	pull down to GND



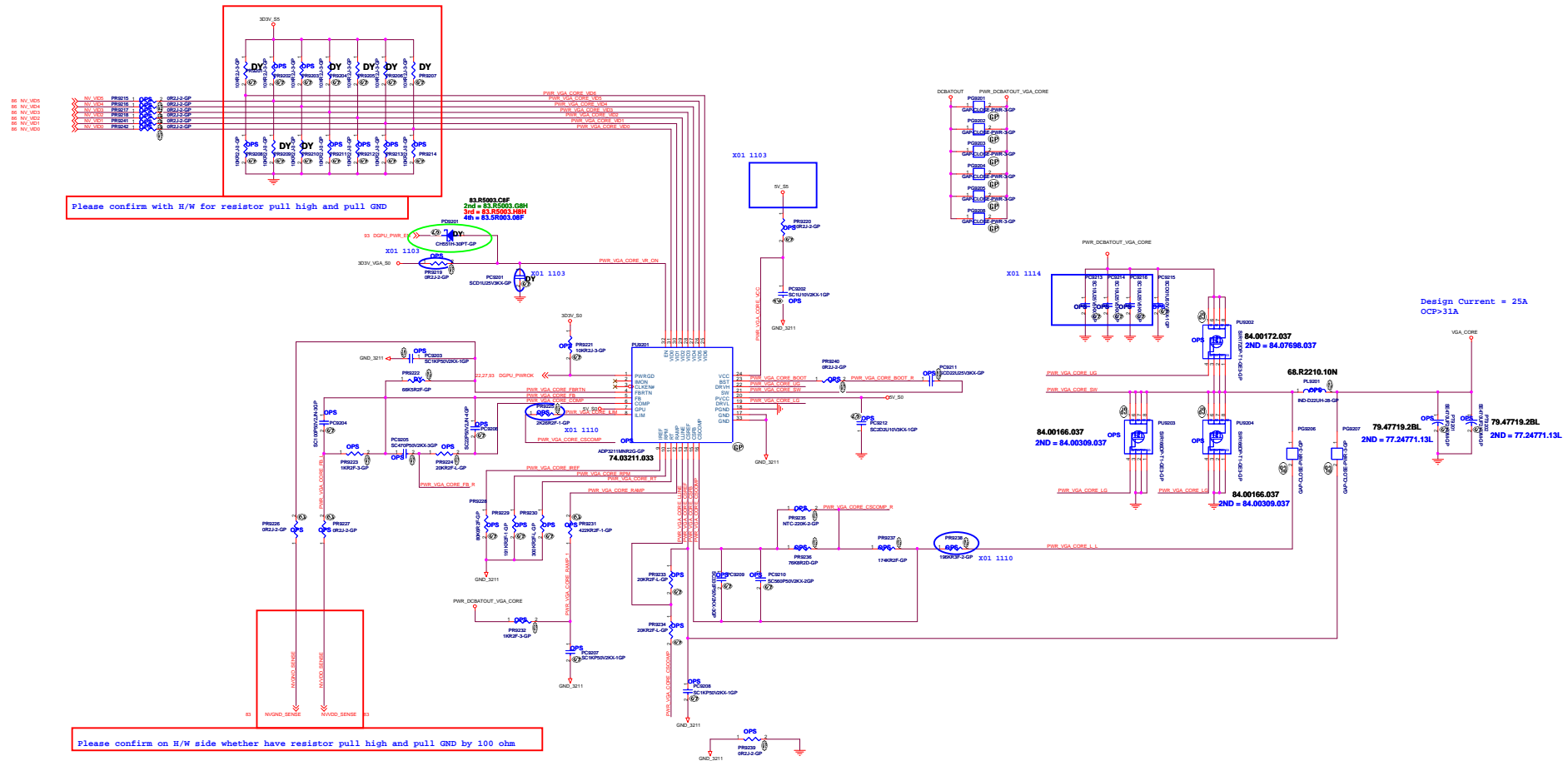
N13x GPUs do not support CEC. Leave the CEC pin as NC

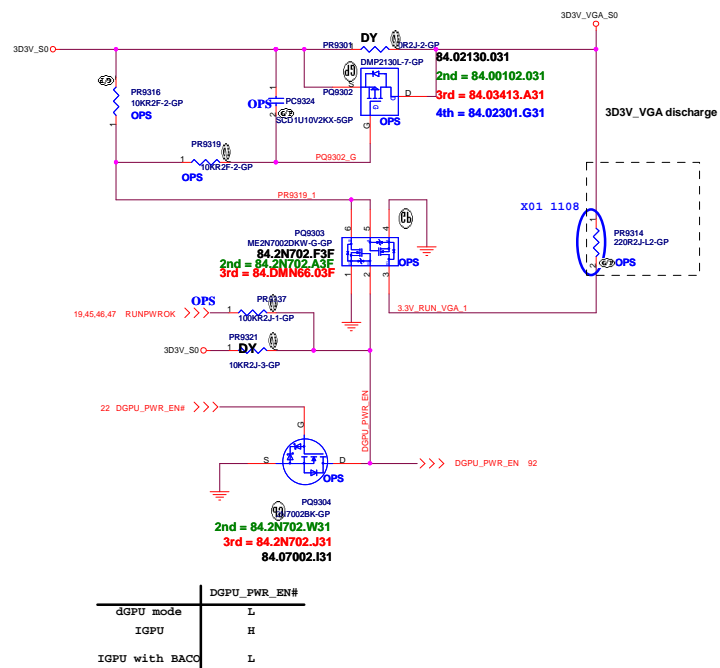






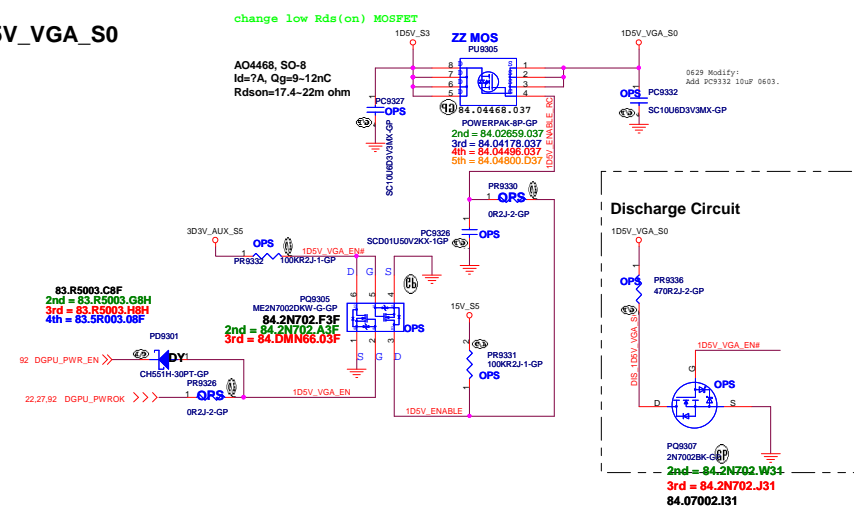
V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.9000V	0	0	0	0	1	1	0





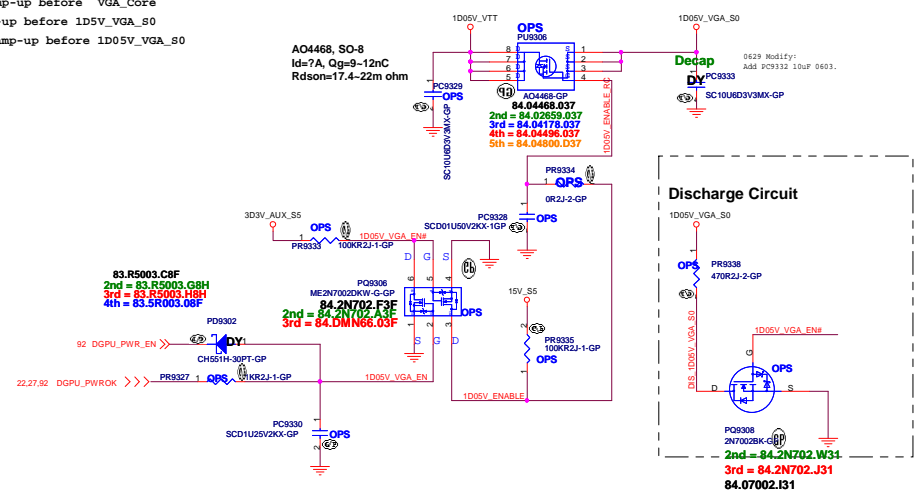
NV do not need 1.8V

1D5V_VGA_S0

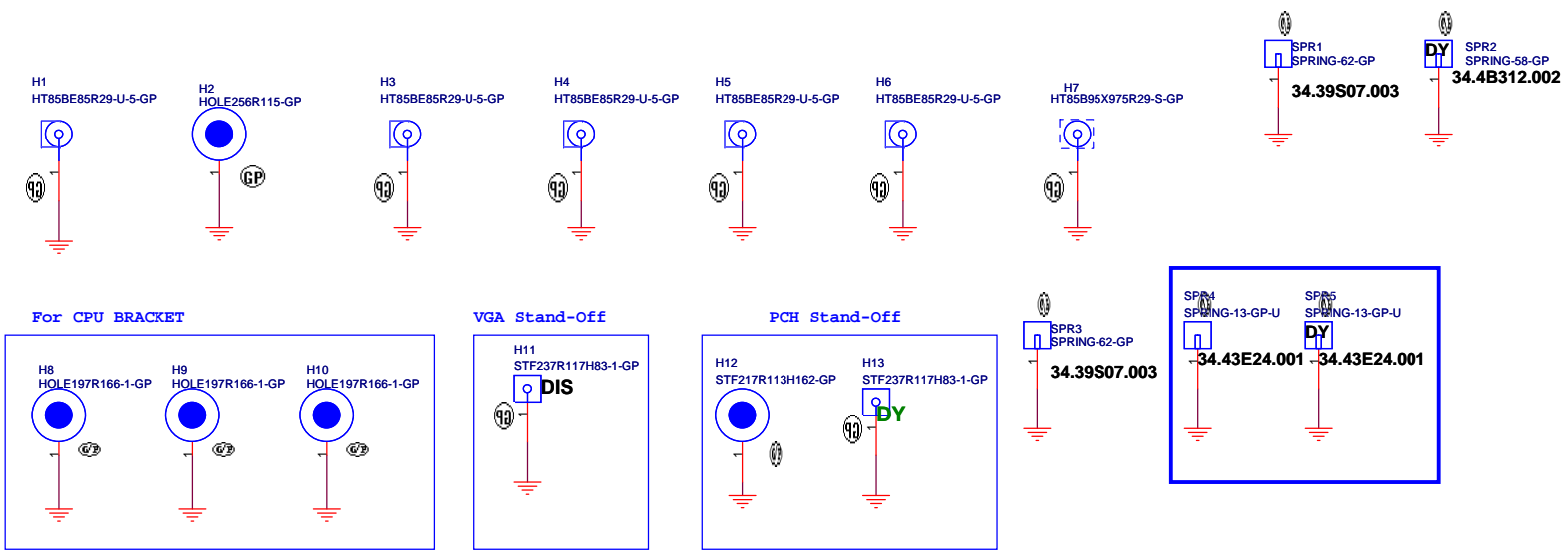


1D05V_VGA_S0

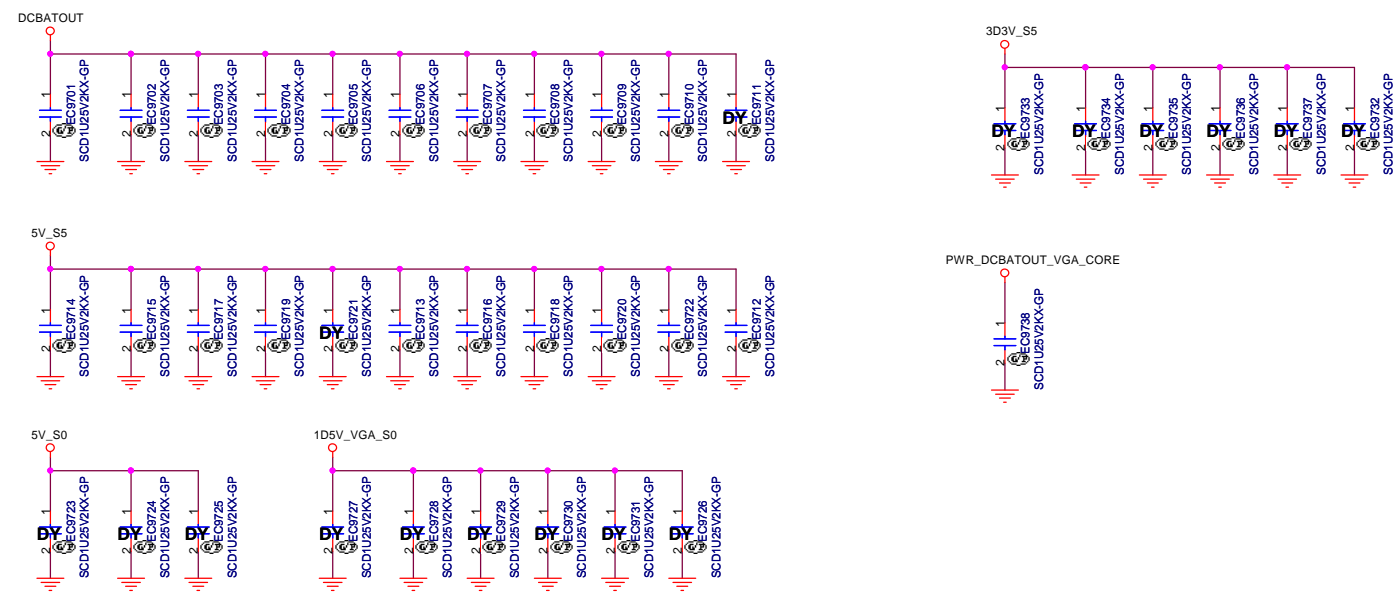
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp-up before 1D05V_VGA_S0



SSID = Mechanical



SSID = EMI



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

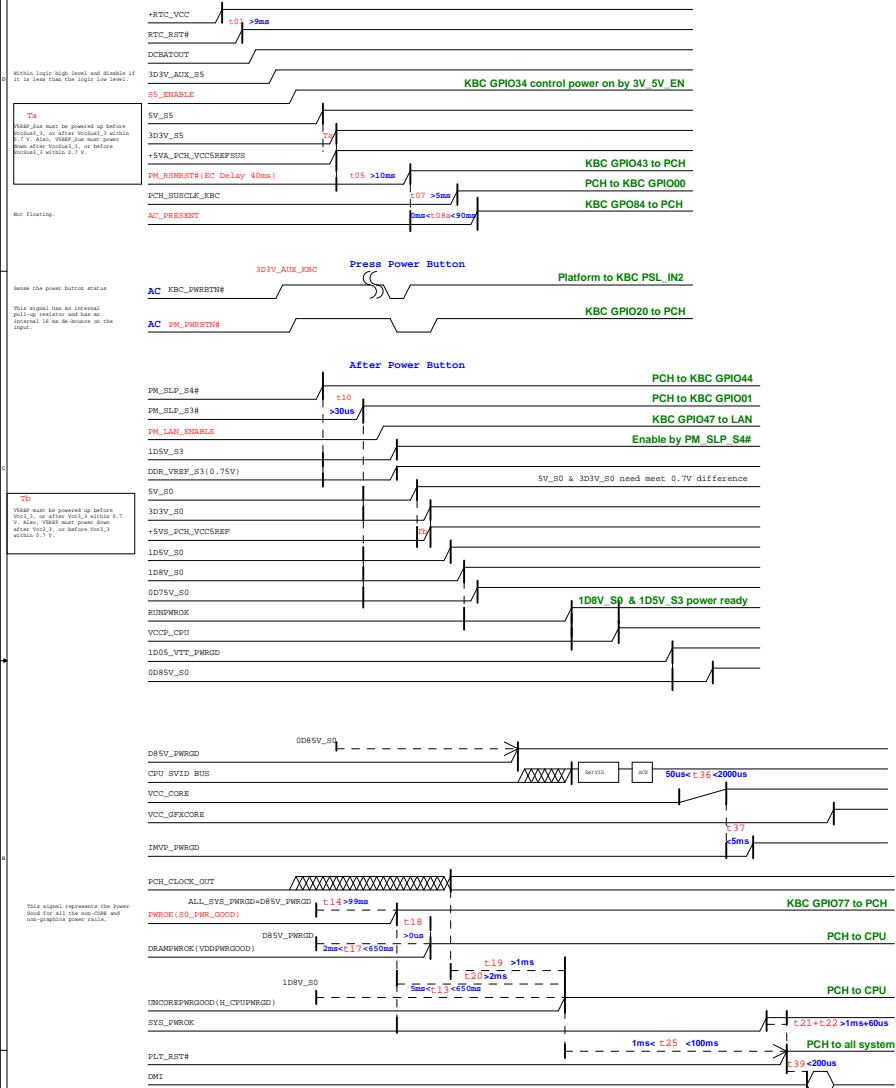
Title
UNUSED PARTS/EMI Capacitors

Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02
Date: Friday, December 30, 2011	Sheet 97	of 104

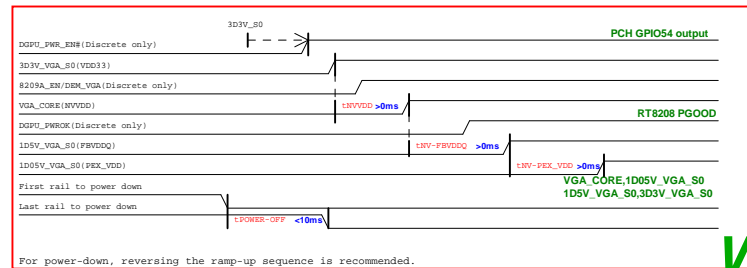
Chief River Platform Power Sequence

(AC mode)

Red Words: Controlled by EC GPIO

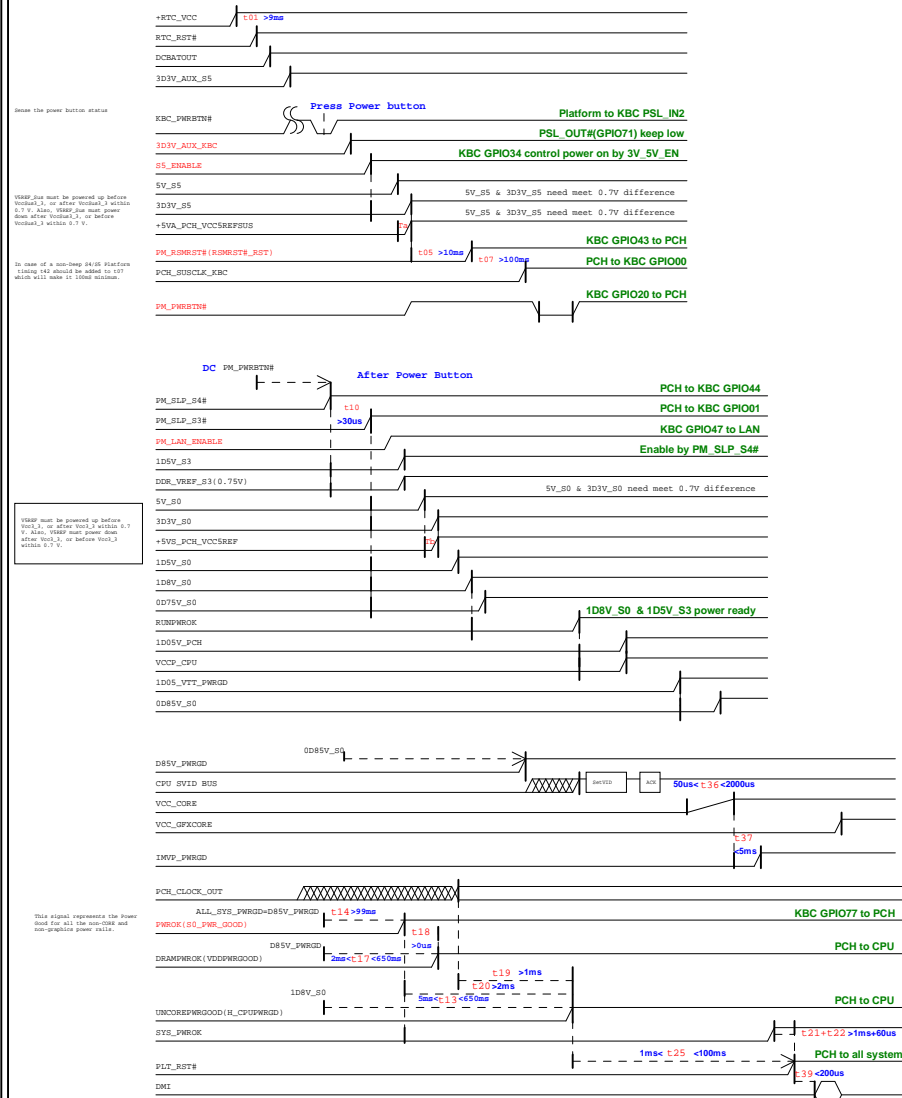


N13M-GS Power-Up/Down Sequence

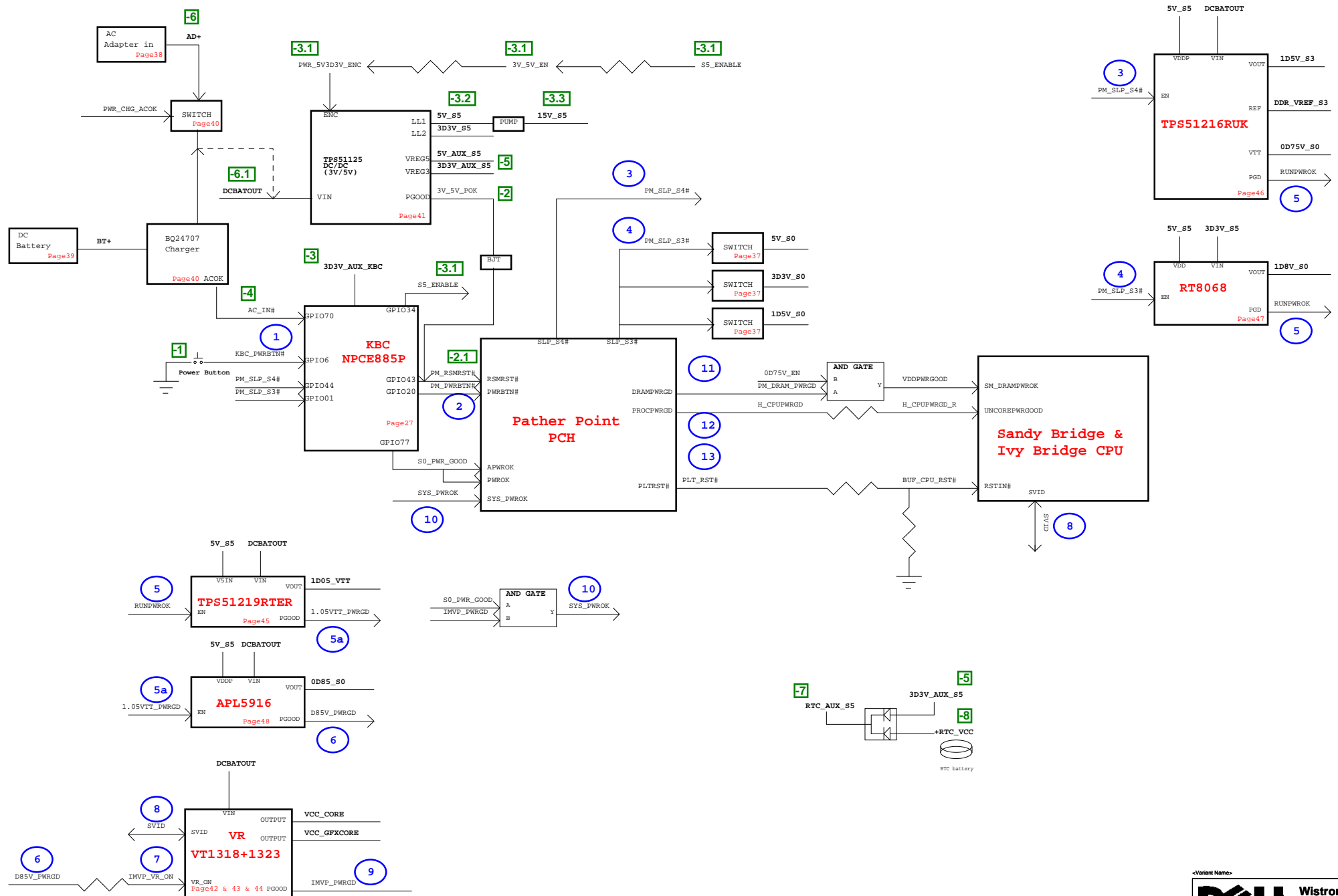


(DC mode)

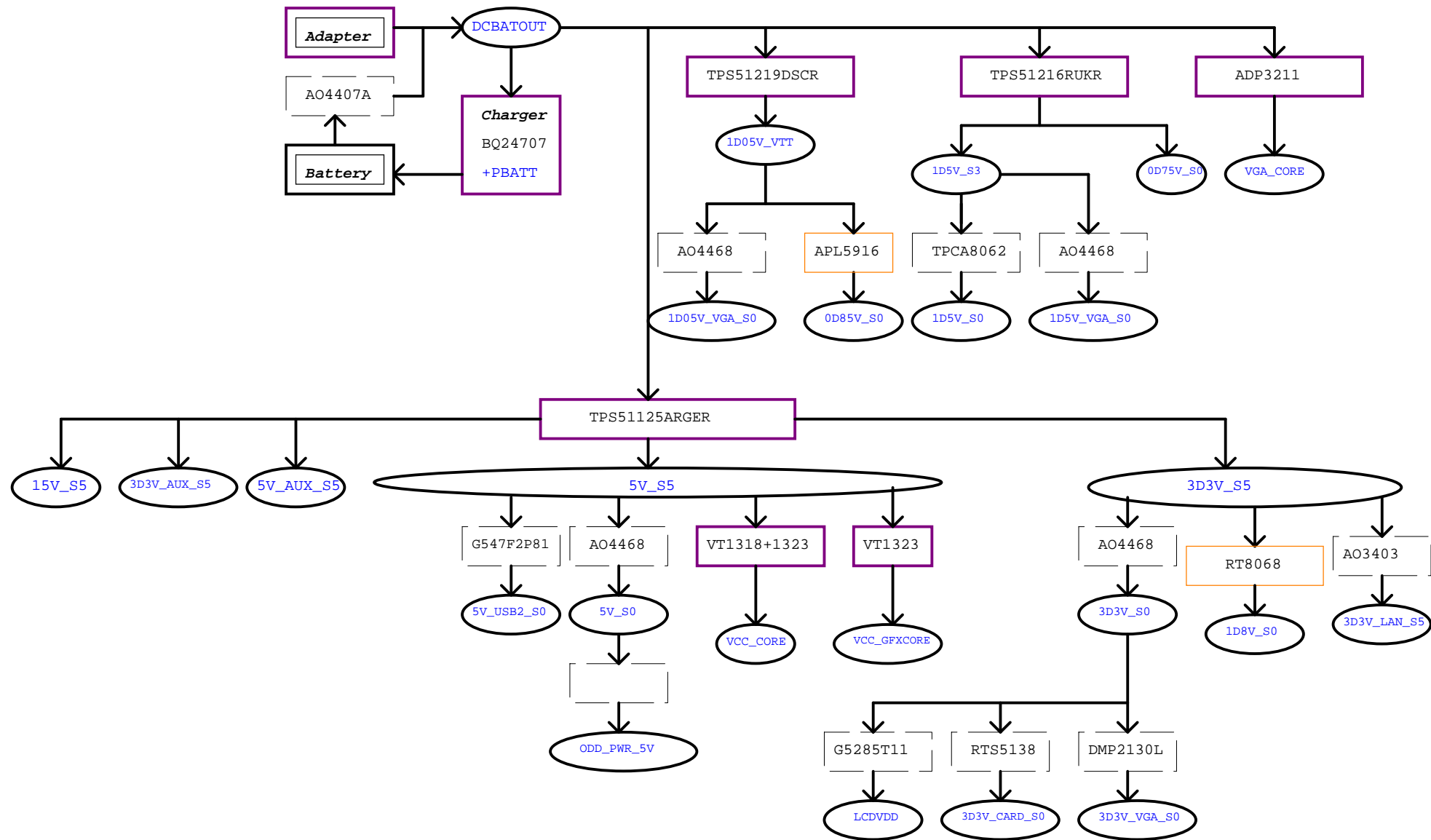
Red Words: Controlled by EC GPIO



DV14 MLK Chief River POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13



Power Shape

Regulator

LDO

Switch

<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

Size
A3

Document Number

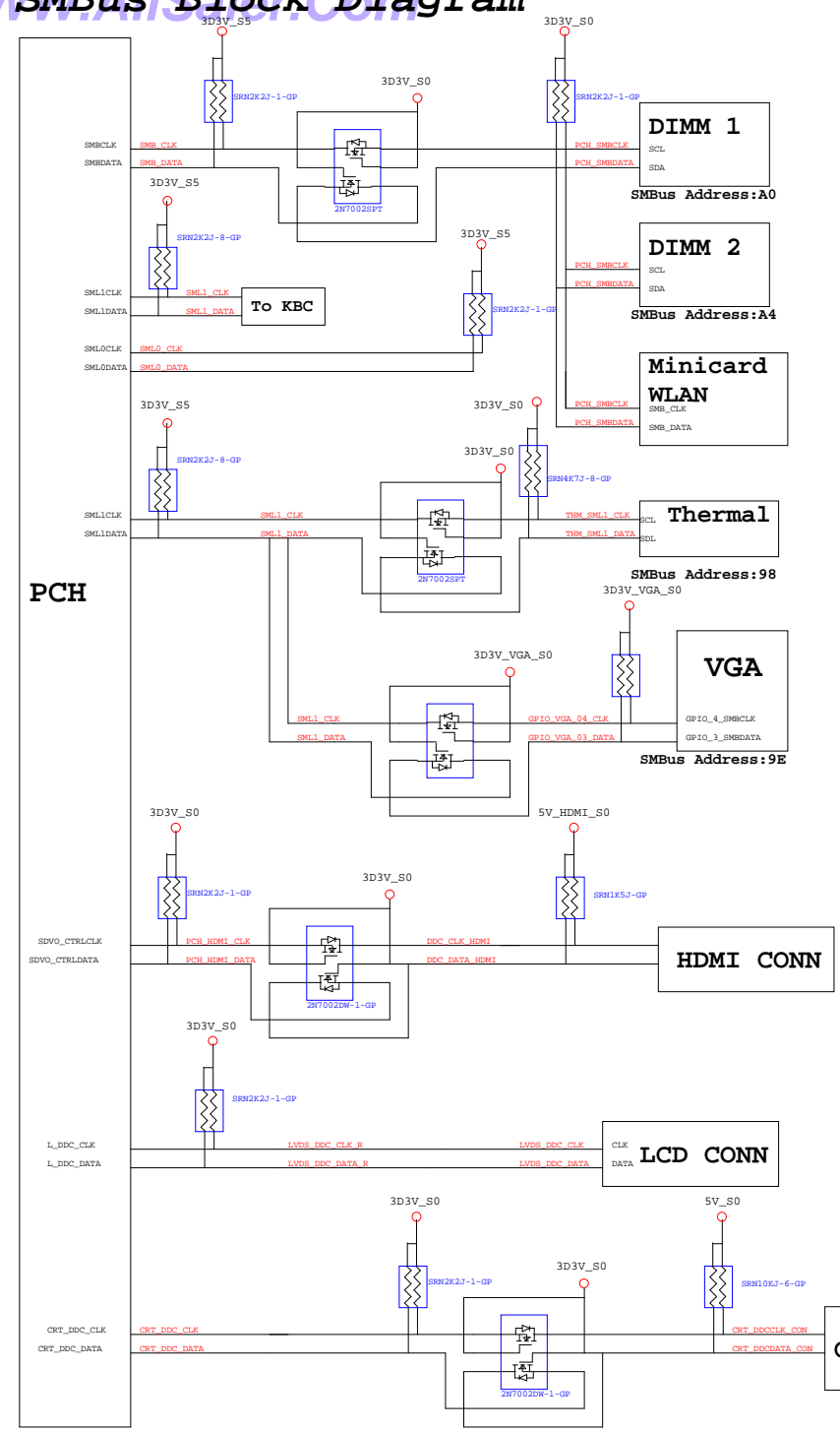
Enrico Caruso 14 MLK DIS

Rev
X02

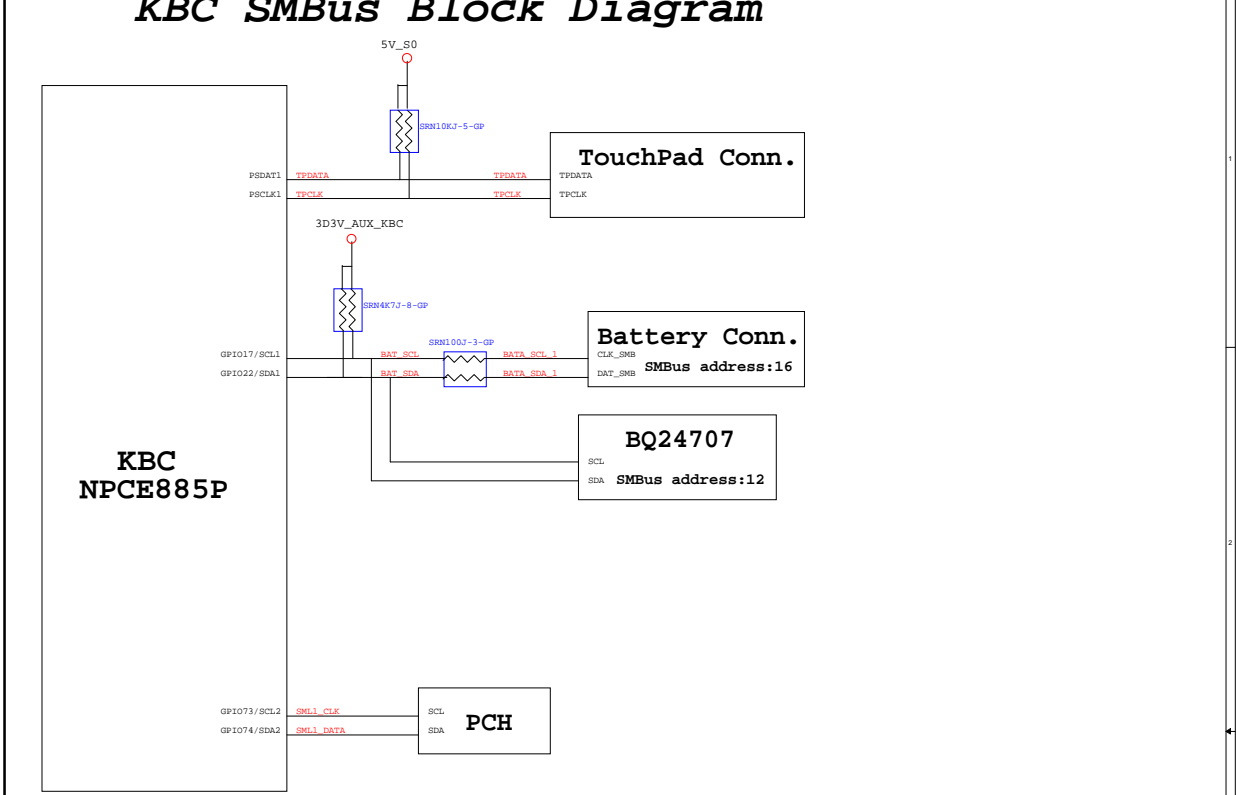
Date: Friday, December 30, 2011

Sheet 100 of 104

PCH SMBus Block Diagram



KBC SMBus Block Diagram






The diagram illustrates the connections of the **Codec 92HD79B1** to various external components. The codec is represented by a large blue rectangle on the left. Connections are shown as lines extending from the codec to specific components on the right, which are represented by colored rectangles.

- SPEAKER** (Pink rectangle): Connected to `SPKR_PORT_D_L-` and `SPKR_PORT_D_R+`.
- HP OUT** (Light blue rectangle): Connected to `HP1_PORT_B_L` and `HP1_PORT_B_R`.
- MIC IN** (Light green rectangle): Connected to `HP0_PORT_A_L`, `HP0_PORT_A_R`, and `VREFOUT_A_OR_F`.
- Digital MIC** (Light orange rectangle): Connected to `DMIC_CLK/GPIO1` and `DMIC0/GPIO2`.
- Analog MIC** (Light purple rectangle): Connected to `PORTC_L`, `PORTC_R`, and `VREFOUT_C`.

VERSION	DATA	PAGE	Change Item
X01	11/03	92	change PU9201 pin24 from 5V_S0 to 5V_S5 to avoid 5V_S0 leakage issue
	11/03	92	change PR9219 from 10K to 0ohm and DY PC9201 to adjust VGA_CORE sequence
	11/03	93	change PR9314 from 470 ohm to 220ohm to adjust 3D3V_VGA_S0 power down sequence
	11/08	40	change PC4010 from 78.47422.2QL to 78.47422.2BL to correct wistron Part number
	11/08	86	change VGA strap pin follow NV FAE suggest
	11/08	42	change PR4120 from 10K to 9.76K to adjust 5V_S5 from 5.0V to 5.07V
	11/09	36	change R3605 from 10K to 0 ohm,R3607 and R3630 from 10K to 100K, C3610 from 0.01 uF to 0.047 uF to adjust 3D3V_S0, 5V_S0 and 1D5V_S0 power sequence
	11/09	17	change RN1703 from 33 ohm to 22 ohm to solve CRT HSYNC and VSYNC rise and fail time issue
	11/09	50	change L5001 L5002 L5003 to 68.00084.931 to solve CRT RGB rise and fall time fail issue
	11/09	40 38 97	stuff EC4002,EC9709,EC9701,EC9705,EC9708,EC9702,EC9703,EC9704,EC9738,EC9710,EC4001,EC9707,EC9713,EC9715,EC9716,EC9720,EC9718,EC9712,EC9714,PC4120,EC9717,EC9719,EC9722,PC3801,EC9706,SPR1,SPR3,SPR4 for EMI request
	11/09	27	change R2724 from 10K to 20K for PCB version change
	11/09	86	change ROM_SLK_D4 to SMB_ALT_ADDR follow NV Design Guide
	11/09	86	change ROM_SO_C4 to VGA_DEVICE follow NV Design Guide
	11/09	86	change ROM_SI_D3 to SUB_VENDOR follow NV Design Guide
	11/09	86	change STRAP0_STRAP3 to RAM_CFG[0]_RAM_CFG[3] follow NV Design Guide
	11/09	86	change STRAP4 to PCIE_MAX_SPEED follow NV Design Gide
	11/10	22 83	dummy R8319 R8307 R2205 stuff U8301 and add R2202 to pull high DGPU_HOLD_RST# to 3D3V_S0 follow NV FAE suggest
	11/10	21	seperate RN2203 to R2205 and R2206 for bom control
	11/11	41	change PR4102 from 51K to 61.9K to set 5V OCP
	11/11	41	change PR4101 from 120K to 91K to set 3.3V OCP
	11/11	42	change PR4236 from 1.78K to 2.05K for CPU Loadline adjustment
	11/11	42	change PR4264 from 20K to 18.2K for CPU Loadline adjustment
	11/11	42	change PR4239 from 0 ohm to 191 ohm for GFX Loadline adjustment
	11/11	42	change PR4249 from 7.87K to 7.5K for GFX Loadline adjustment
	11/11	46	change PR4602 from 52.3K to 80.6K to Set 1.5V OCP
	11/11	92	change PR9238 from 133K to 196K and PR9225 from 3.83K to 2.26K for Loadline adjustment follow Nvidia SPEC
	11/11	45	dummy PR4506 and PR4507, Pop PR4505 and 3D3V_S0 change 3D3V_S5 for power team request
	11/11	29	install R2909,R2910,D2902 as to audio chip will change to 4213D
	11/14	92	change PC9213 PC9214 PC9216 to 78.10622.51L for power team request
	11/15	29	change R2909 R2910 to 0 ohm for vendor request
	11/15	61 82	stuff TR8201 TR8202 TR6101,dummy R6102 R6203 R8201 R8202 R8203 R8204 for EMI request
	11/16	39	add test point AFTP3902

VERSION	DATA	PAGE	Change Item
X01	11/16	31	change C3102 C3103 to 15pF for vendor suggest
	11/16	86	change C8610 C8611 to 10pF for vendor suggest
	11/23	88 89	change R8807 R8908 from 80.6 ohm to 162 ohm for NV FAE suggest
	11/24	83	change L8302 to 0 ohm for NV FAE suggest
X02	12/16	20	reserve R2005 10K Pull High for PEG-CLKREQ#_L
	12/16	29	change R2945 to 2.2K,accuracy 'J' follow vendor suggestion to solve internal mic too low issue
	12/22	88	DY C8815 C8816,stuff C8809 to avoid HDD interfere.
	12/23	22	DY R2202,stuff R2205 to pull low DGPU_HOLD_RST# to follow NV Design Guide
	12/23	20 83	DY R2004,stuff R2005 to pull high PEG_CLKREQ# to 3D3V_S5,stuff R8302 to pull high VGA_PEG_CLKREQ#,stuff Q8301 follow NV suggestion
	12/27	28	exchange the name of AFTP2801 and AFTP2802 to stay same with UMA for AFTP request
	12/28	40	add 0.1uF caps EC4004(BT+_R to GND) and EC4003(PWR_DCBATOUT_CHG to GND) to reduce EMI noise
	12/28	27	change R2724 from 20K to 33K for PCB version change
	12/29	88	remove C8815 to avoid HDD interfere follow NV suggestion
	12/29	32 51 65	changed R3206,R3207 to short pad,removed TR3201 CMC footprint;changed R5101,R5102,R5103, R5104,R5105,R5106,R5107,R5108 to short pad,removed TR5101,TR5102,TR5103,TR5104,CMC footprint;changed R6505,R6506 to short pad,removed TR6501 CMC footprint follow EMI suggestion
	12/29	5 14 15 18 19 23 24 27 28 29 31 32 36 37 44 46 51 65 68 83 86	change R504 R1404 R1405 R1503 R1504 R1807 R1906 R1910 R1912 R1913 R1924 R1929 R2306 R2307 R2308 R2402 R2403 R2404 R2720 R2723 R2761 R2764 R2765 R2766 R2767 R2768 R2778 R2792 R2794 R2807 R2813 R2905 R2906 R3105 R3208 R3605 R3614 R3708 R3710 R5101 R5102 R5103 R5104 R5105 R5106 R5107 R5108 R5125 R6505 R6506 R6510 R6511 R6804 R6805 R6811 R6813 R8503 R8607 / L8302 L8601 R2304 R2412 R3104 R3115 R3117 R3206 R3207 R4908 / R2301 R2911 R2912 / RN2010 RN2012 RN2014 RN2016 RN5002 / PR4212 PR4116 PR4121 PR4127 PR4252 PR4254 PR4251 PR4250 PR4261 PR4220 PR4232 PR4244 PR4304 PR4305 PR4403 PR4611 PR4607 from 0ohm to short pad
	12/29	58	change EC5801 EC5802 EC5803 EC5804 to 1000P cap for EMI request
	12/30	29	add 100K R2913 resistor in AUD_PC_BEEP let voltage can be discharged fast
	12/30	61 82	remove R6102,R6103;R8201,R8202;R8203,R8204 co-lay position;use CMC solution
	12/30	27	change R2735 from 10K to 20K to reduce inrush current of 3D3V_AUX_KBC
	12/30	41	change PC4126,PC4127 to 4.7u from 10u follow power team's suggestion
	12/30	27 86	remove TP2713,add R2713 for pull high OVER_CURRENT_P8# to 3D3V_AUX_KBC;add R8608,Q8603; change Q8603.2 to OVER_CURRENT_P8# from AC_PRESENT for OC trigger IPCC function
	12/30	58	stuff 1000pf EC5801 EC5802 EC580 EC5804 for EMI request
	01/03	49	remove R4903,R4904 co-lay position;use CMC solution
	01/03	45	change PR4510 to 82.5K from 69.8K to modify OCP follow power team's suggestion

<Core Design>

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File			
Change History			
Size A3	Document Number Enrico Caruso 14 MLK DIS	Rev X02	
Date: Wednesday, January 04, 2012	Sheet 103 of 104		

